CS/ECE 347, Spring 1996

Recitation Assignment 10: Memory Hierarchy

Assigned: Tue., Apr. 16

Due: Mon., Apr. 22

Memory Hierarchy

The following series of problems concern a hierarchical memory structure with the following features:

- The memory is byte addressable.
- Virtual addresses are 16 bits wide.
- Physical addresses are 14 bits wide.
- The page size is 128 bytes.
- The TLB is 4-way set associative with 16 total entries.
- The cache is direct mapped, with a 4 byte line size and 16 total lines.

In the following tables, all numbers are given in hexadecimal. The contents of the TLB are as follows. Note: Despite the labels in the figure, each 4-way set occupies a row in the table.

TLB

Index	Set 0			Set 1			Set 2			Set 3		
	Tag	PPN	Valid	Tag	PPN	Valid	Tag	PPN	Valid	Tag	PPN	Valid
0	02	13	1	04	32	1	00	28	1	01	0C	0
1	03	2A	1	01	37	0	02	0A	0	02	0C	1
2	01	38	0	00	18	1	08	01	0	03	11	1
3	05	2B	1	04	1A	1	0D	07	0	01	10	1

The page table for the first 16 pages, and the cache contents are as follows

Page Table (Partial)

VPN	PPN	Valid	VPN	PPN	Valid
000	28	1	008	13	1
001	42	0	009	0C	1
002	18	1	00A	07	1
003	0B	1	00B	24	0
004	0C	0	00C	05	0
005	0B	0	00D	2A	1
006	43	1	00E	11	1
007	10	1	00F	11	0

Cache

Index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	19	1	99	11	23	11
1	15	0	55	59	0B	41
2	13	0	12	E2	89	A4
3	22	1	3A	DD	83	11
4	20	1	45	48	0C	A1
5	22	1	23	99	8E	BB
6	2E	0	29	90	E2	59
7	16	1	62	0C	FF	22
8	22	1	5D	13	E3	49
9	13	1	0D	2B	02	3F
A	1F	1	89	38	F4	CC
B	C4	0	40	A7	05	6F
C	B1	1	38	5F	B1	A4
D	26	1	A7	31	37	F8
E	99	0	0D	0C	52	19
F	51	1	88	96	0B	D8

Problem 1. (5 points):

A. The box below shows the format of a virtual address. Indicate (by labeling the diagram) the fields that would be used to determine the following:

VPN The virtual page number

VPO The virtual page offset

TLBI The TLB index

TLBT The TLB tag

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. The box below shows the format of a physical address. Indicate (by labeling the diagram) the fields that would be used to determine the following:

PPN The physical page number

PPO The physical page offset

CO The byte offset within the cache line

CI The cache index

CT The cache tag

13	12	11	10	9	8	7	6	5	4	3	2	1	0

For the following problems, you are to show how the memory translates a virtual address into a physical and accesses the cache. For the given virtual address, indicate the TLB entry accessed, the physical address, and the cache byte value returned. Indicate whether the TLB misses, whether a page fault occurs, and whether a cache miss occurs. Carry each translation as far as possible, i.e., until there is insufficient data to complete the translation. Mark '—' through entries that cannot be correctly determined.

Problem 2. (5 points):

Virtual address `04C1`

A. Virtual address format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	

Problem 3. (5 points):

Virtual address `02F0`

A. Virtual address format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	

Problem 4. (5 points):

Virtual address `0569`

A. Virtual address format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	
TLB Index	
TLB Tag	
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	

C. Physical address format

13	12	11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Byte offset	
Cache Index	
Cache Tag	
Cache Hit? (Y/N)	
Cache Byte returned	