CS/ECE 347, Spring 1996
Recitation Assignment 8: Cache basics

Assigned: Thu., Apr. 5
Due: Mon., Apr. 8

1. Problem 1

Consider an address space of 128 byte-addresses and a cache with 32 total data bytes and a line size of 4 bytes. Complete the following table for the different kinds of cache organizations:

	direct mapped	2-way set assoc	4-way set assoc	fully assoc
n (# address bits)				
t (# tag bits)				
s (# set index bits)				
b (# block offset bits)				
S (# sets)				
E (# entries/set)				

2. Problem 2

Assume the address space, cache size, and line size from Problem 1. For each of the following addresses, indicate (1) the set number that the address is mapped to in the cache and (2) the corresponding tag bits.

	direct mapped		2-way set assoc		4-way set assoc		fully assoc	
address	set	tag bits	set	tag bits	set	tag bits	set	tag bits
25								
75								
90								