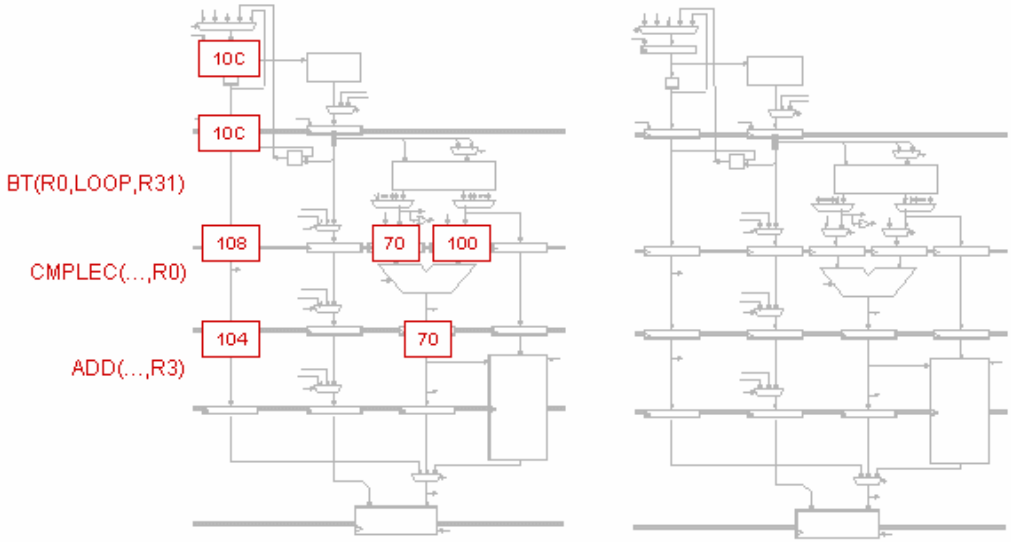
Daniel Leeds, R20, May 5, 2006

B. **Scenario 2**: assume R1 contains 10, R2 contains 60

```
. = 0x100
LOOP: ADD(R1,R2,R3)
      CMPLEC(R3,100,R0)
      BT(R0,Loop,R31)
      SHLC(R3,1,R3)
```



Problem 1:

A In a 5-stage pipelined Beta, when does the hardware use its ability to insert NOP into the instruction stream at the IF stage

E Which of the following cannot be dealt with transparently and at no performance cost by bypassing?

A A shared register between consecutive ALU instructions.
B A BR followed by an ALU instruction using the BR.
C An LD followed by an ALU instruction using the LD.
D Access to LP by the first instruction in a called procedure.
E Access to XP by the first instruction in an interrupt handler.

Problem 2:

```
loop: LD(R31, status, R0)
      BEQ(R0, loop, R31)
      ADD (R0, R1, R2)
```

IF	LD	BEQ	ADD	ADD	ADD	LD	BEQ	ADD	ADD	ADD
REG		LD	BEQ	BEQ	BEQ	NOP_3	LD	BEQ	BEQ	BEQ
ALU			LD	NOP_1	NOP_2	BEQ	NOP_3	LD	NOP_4	NOP_5
MEM				LD	NOP_1	NOP_2	BEQ	NOP_3	LD	NOP_4
WB					LD	NOP_1	NOP_2	BEQ	NOP_3	LD

	i	i+1	i+2	i+3	i+4	i+5	i+6	i+7	i+8	i+9	i+10	i+11
IF												
RF												
ALU												
Mem												
WB												

	i	i+1	i+2	i+3	i+4	i+5	i+6	i+7	i+8	i+9	i+10	i+11
IF												
RF												
ALU												
Mem												
WB												

	i	i+1	i+2	i+3	i+4	i+5	i+6	i+7	i+8	i+9	i+10	i+11
IF												
RF												
ALU												
Mem												
WB												

	i	i+1	i+2	i+3	i+4	i+5	i+6	i+7	i+8	i+9	i+10	i+11
IF												
RF												
ALU												
Mem												
WB												

	i	i+1	i+2	i+3	i+4	i+5	i+6	i+7	i+8	i+9	i+10	i+11
IF												
RF												
ALU												
Mem												
WB												