Towards a Reconfigurable Nanocomputer Platform

Paul Beckett

School of Electrical & Computer Engineering, RMIT University
124 Latrobe St., Melbourne, Australia, 3000
pbeckett@rmit.edu.au

Abstract

Some ideas are presented for achieving low-overhead reconfigurability in systems built from nanoscale components. Via three example circuits, it is demonstrated how it will be possible to exploit a number of alternative "dimensions" – apart from the obvious spatial dimension - to construct compact configurable cells. Configurability based on dual gate transistors using RTD-based multi-valued logic and the variable resistance of phase-change films are shown. A high-density non-volatile reconfigurable cell is proposed in which a double junction spin filter tunnel junction is built on a vertical conducting pillar and integrated into a nearest neighbour-connected mesh. Some brief comments are made about how computing applications might exploit such a homogenous non-volatile processing mesh.

1 Introduction

Reconfigurable architectures are of great interest to system designers because they offer a way of achieving power and performance efficiency by matching algorithmic constructs with the appropriate architectures [1]. The traditional approach to reconfiguration, in FPGAs for example, has been to build separate areas of programmable logic gates and interconnection blocks from transistors and to manage the two resources more-or-less separately during the synthesis process. Much of the work on constructing reconfigurable platforms has therefore been directed towards answering the questions "how much of each and in what form?" [2], [3]. This is largely because reconfiguration is expensive – it increases the area and power requirements, while reducing the performance of a system compared to purpose-built solutions[1]. It also places constraints on the solution space accessible to the synthesis process that are unique to the particular platform, reducing the generality of system solutions. Achieving optimum performance in a reconfigurable system by striking a balance between logic and interconnect is often difficult.

The continued scaling of devices into the deep-sub-micron region will have a number of consequences for reconfigurable systems. For example, it appears likely that only arrays of simple cells with highly localised interconnect will be available. This will be the inevitable result of the reduced fanout, power handling capacity, gain and reliability of DSM devices. Thus it is likely that the boundaries between logic and interconnect will become increasingly difficult to identify.

On the other hand, as a result of scaling novel circuit techniques are becoming available: vertically integrated and thin-film based transistors, heterogenous resonant tunnelling devices, single-electron quantum dots and spin filter devices to name just a few.

This paper addresses the basic question: how can low-overhead reconfigurable systems be built with nanoscale technology? It is proposed that the answer to this question is really the same as that for achieving high fabrication density – to exploit the "3rd dimension" wherever available.

The use of aggressive vertical integration is resulting in some extremely compact circuits (e.g. [5]) and 3D or spatially stacked techniques promise to increase this significantly [6]. However, this is not the only "dimension" available. High density, high functionality configurable building blocks can also be achieved by simultaneously exploiting a number of available physical variables (voltage, current, threshold voltage; magnetic field, electron spin, etc).

Three plausible configurable building blocks will be described that illustrate how this might be achieved. In Section 2, an example is presented of how transistor logic scaled into the nanometer domain can be combined with RTD-based multi-valued logic to support fine-grained configurability. A second example, in Section 3, exploits the characteristics of phase transition thin-films and vertical integration to reduce the size of the cell and at the same time support non-volatile operation. In Section 4, a cell based on magnetic tunnelling technology is described that exploits a number of physical variables to merge logic and configuration

---

[1] This has been stated as the "Law" of FPGAs vs. ASICs: *"for any FPGA-based application, there is an ASIC implementation of the system that is AT LEAST as fast, dense, power-efficient, and cheap in (very) high volumes as the FPGA based solution"* [4]

into a single space. The fabrication of these building blocks will not be described in exhaustive detail. Rather, the intention is to explore how the particular techniques might offer high functionality within dense structures.

Finally, Section 5 briefly outlines a general direction that computing applications might take on such a homogenous non-volatile processing mesh.

2 A Multi-valued SRAM Based Platform

This example mesh brings together the Resonant Tunnelling based multi-valued SRAM described in [7] and more recently in [8] and [9], the metal-insulator tunnel transistor (MITT) [10], [11] and a some of the 3D interconnection ideas described, for example, in [12], [13] and [14]. The resulting structure forms a large planar logic mesh of simple (2-input) logic gates in two of its dimensions, which can be configured into a interconnected logic structure via a vertically stacked (multi-valued) RTD-based RAM array.

Although their characteristics are similar, the MITT device [10] operates quite differently to a standard FET. The gate voltage modulates the tunnel barrier thickness, changing the Fowler-Nordheim tunnelling currents that flow through the metal/insulator junction. In the proposed device (Figure 1), a second (back) gate has been added so that the tunnelling current becomes a function of both. A number of dual-gate transistors have been described (e.g. [15], [16], [17], [18]) but none based on MITT technology[2]. This idea has the advantage that the all-metal devices are compatible with current fabrication processes and can be easily extended to multi-layer 3D topologies.

Accessing the two gates independently allows the upper gate to be used to set the operating point of the transistor – effectively setting the threshold voltage of the lower gate that provides the logic connection. By setting the transistor bias points appropriately, a logic gate can be built that exhibits three operating regions (Figure 2) – always on (V_{G1}>0.1), always off (V_{G1}<-0.4) and inverting operation with a logic swing of 0.4V (-0.2 <V_{G1}< -0.1). The top-gate voltage V_{G1} will become the reconfiguration voltage for the homogenous logic mesh.

The 3-state memory cell proposed by Wei et al [7] and more recently by van der Wagt [8] provides a useful mechanism for generating the three threshold voltages required. The basic memory cell is redrawn in Figure 3 along with its (idealised) load-line curves.

---

[2] the back-gate is not intrinsically necessary in this case as the operation would be the same with any dual-gate transistor. The back-gate makes the cell layout denser.

To merge this into the processing mesh will involve matching the V_{G1} values required to set the MITT into its three operating domains with the RTD tunnelling voltages V_{1-3} which are set, in turn, by adjusting the (AlAs) barrier thicknesses of both RTDs [19].

The top gate connections form the contact point to the RTD memory cells. In the configuration shown, memory cells are paired with each pair setting the configuration for the two-input NOR gate below. The cell layout depicted in Figure 5 is based on a similar layout described in [8] and illustrates how the heterojunction RTDs might be assembled on a substrate grown over an insulator layer containing the MITTs.
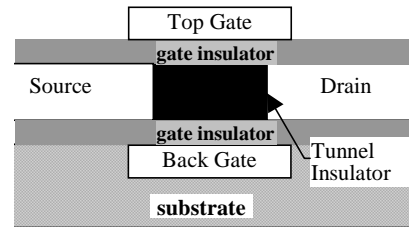

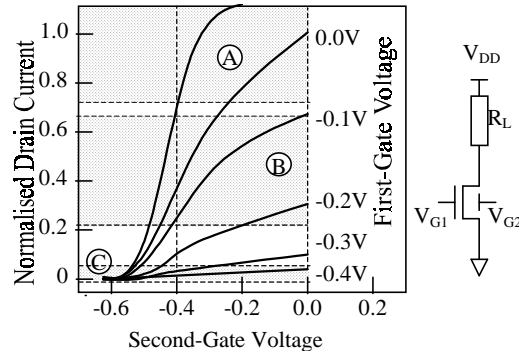**Figure 1** Proposed Double-Gate Metal Insulator Tunnel Transistor

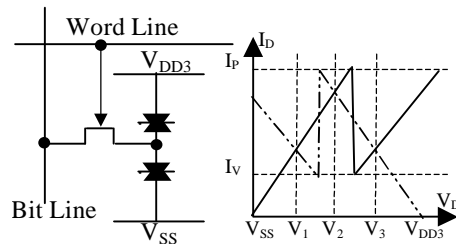**Figure 2** Typical Dual Gate Transfer Characteristics

Figure 3 RTD-Based SRAM Cell (from **[7]**)

A major problem with RTDs is the need to closely control the growth of the tunnelling layers as the tunnelling current depends exponentially on the tunnel barrier thicknesses. For large scale integration III/V technology appears to be the most promising,

although a number of significant processing challenges remain [20]. At present the integration density is limited by the minimum lateral feature sizes for RTD devices (about 1 µm) and their operating currents (peak currents are about 5mA). The Nanotechnology Roadmap [20] predicts that they will scale to about 200nm by 2006 and around 50nm by 2012. At this point, these RTD-based memory cells could be built with dimensions down to about 300nm x 100nm, and the MITT based logic cells should scale to ~10nm gate lengths. This represents a density in the order of 3×10^9 cells/cm^2, or the equivalent of about 10^9 2-input gates/cm^2.
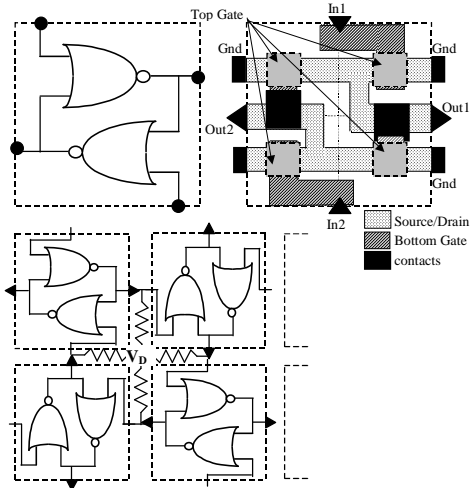

Figure 4   An Example Logic Cell, Layout and Tiling
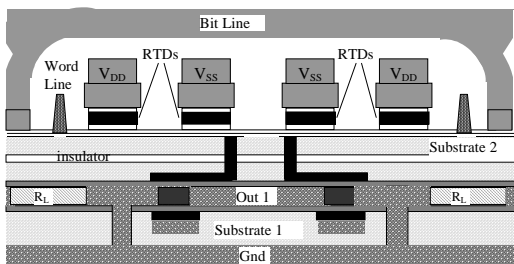

Figure 5   Vertically Integrated Logic Cell Structure

3   Phase Transition Devices

Phase transition RAMs generally comprise layers of chalcogenide semiconductor thin-films (containing at least one group-VI element) and use a reversible structural phase change as the storage mechanism. The memory cells act as a fast programmable resistor that can be programmed by the application of a current pulse. Phase transition technology has been in use for a number of years in non-volatile applications such as optical disks and more recently phase-transition RAM have been proposed [21], [22].

For optical disk applications, the difference in optical characteristics between the crystalline and amorphous states defines the logic state of an individual cell, whereas for RAM applications it is the resistance of the film that is measured [23].

The chalcogenide alloy material is compatible with current (CMOS) logic fabrication, adding only 2 - 4 late, low temperature mask steps to a standard process [24]. The technology scales well as smaller memory cells use less power during the phase change, operate at lower voltages, are less prone to electric field damage and therefore have much greater write/erase lifetimes. Stable operation has already been reported with phase transition areas down to 20nm in diameter [21] and multi-state storage via programming to intermediate resistance values has been demonstrated [24].
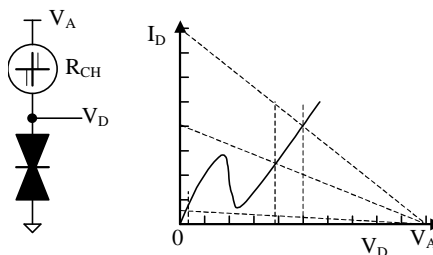

Figure 6   Multi-Valued RTD/Phase-Transition Memory Cell
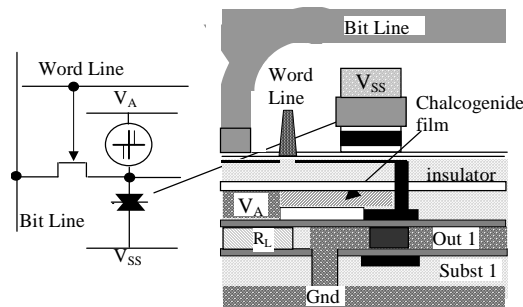

Figure 7   RTD/Phase-Transition Memory Cell Configuration

By using a chalcogenide resistor as the load for a resonant tunnelling diode (Figure 6), it is possible to create a smaller multi-valued RAM cell that is also non-volatile. As shown, the variable resistance of the phase-change film is used to establish the three operating points as before. The design of the cell will involve matching the operating resistances of the chalcogenide material to the V-I characteristic of the RTD, and at the same time minimising the static power dissipation of the configuration cell. This will need to be held at less than 1nW per cell if the potential maximum mesh densities are to be realised in practice.

A possible 3D layout shown in Figure 7 merges the chalcogenide film with the top gate of the MITT. The resulting structure is compact, with a likely final cell size under 150nm square. However, by adopting a conventional (PROM) memory array structure, substituting a schottky diode for the RTD and expanding vertically (Figure 8), the cell can be made even more (laterally) compact. In this configuration (shown in this case on a standard silicon substrate) the schottky diode acts both as current isolation for the memory array and to set the reference point for the logic array. Although a silicon junction is probably simpler to fabricate, GaAs might be a better choice as it broadens the choice of metals that might be used to form the schottky junction. Improved metal-to-metal diode junction technology may even allow the semiconductor substrate to be eliminated entirely.
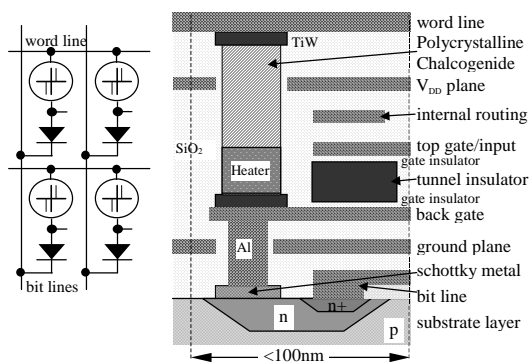

Figure 8   PROM Style Cell Layout

The cell layout as drawn assumes that the chalcogenide film and its resistive heating element can be fabricated as a narrow (e.g. 20-30nm) vertical pillar. The objective is to control the operating resistance of the film and thus manage the static power dissipation of the configuration cell. In Figure 8 the MITT source and drain connections are perpendicular to the page and the vertical connections to ground etc. have been omitted. Seven layers of interconnect metal are used, including the power and ground planes necessary to reduce inductance and cross-talk in the bit and word lines [25].

During normal operation, the word line is held at the reference voltage (V_A in Figure 6) and the bit line at V_{SS} (or ground). Programming a particular bit involves setting the bit/word voltages such that only the bit to be programmed sees a voltage above the transition threshold across the chalcogenide film. As the individual reference/MITT cells can be connected by abutment, with adjacent cells sharing a pull-up device (e.g. a thin-film resistor), this layout will be very compact – gate density could reach the equivalent of 4 x 10^9 reconfigurable 2-input gates per

cm^2. It is also likely that deep trench techniques similar to those used in the S-SGT DRAM device [5], with the non-volatile chalcogenide film replacing the storage capacitance, could reduce the footprint even further.

It is worth noting that this density is achieved at the cost of system level flexibility. Individual bits are no longer programmable while the logic mesh is operating as the bias conditions of the entire mesh needs to be disturbed to program just one bit. This could be partially managed by partitioning the array into separately programmable areas (which might be necessary in any case, due to electrical loading considerations) but this would simply transform the problem into one of deciding the optimum size for these partitions.

Both of these first two examples share a characteristic in common with the majority of current reconfigurable devices such as FPGAs in that the configuration mechanism and the logic mesh occupy completely separate spaces. In this case, unless the mesh layout is augmented to allow for logic plane I/O (for example, by incorporating a separate word/bit read mechanism on additional layers), it would be constrained to the edge of the chip. In the final example that follows, logic and reconfiguration are merged into the same physical space.

4   A Nano-Magnetic Platform

Thin-film magnetic technology seems set to challenge dynamic and non-volatile memories based on conventional semiconductors [26]. For example, Cowburn and Welland [27] have suggested that nano-magnetic technology (Magnetic QCAs, in their case) may eventually support non-volatile active device densities in the order of 2.5 x 10^{11}/cm^2 with a power-delay product that is 10^4 times less than current CMOS.

Magnetic memories are being developed based on the giant magneto-resistive (GMR) effect using devices such as spin-valves and pseudo-spin-valves in which patterned magnetic multi-layers change resistance with changing magnetic moments between the layers [28]. Devices typically comprise two layers of ferromagnetic material separated by a non-magnetic insulator and are "on" (lower resistance) if the direction of magnetization in the two adjacent layers is the same and "off" (higher resistance) if it is in opposite directions. The layers must be narrower than the magnetic domain wall for the effect to emerge, but it remains stable and reproducible with decreasing geometries [29]. However, only a very limited effect has been achieved to date with reported ΔR values ranging between 18% and 40% at room temperature. This is adequate for non-volatile RAM applications in which the resulting small voltage

changes can easily be detected. GMR-based logic has been proposed [30] but its operating currents are still much too large for high density integration.

An alternative magnetoresistive tunnel device has been suggested [31] that has a potential GMR many time larger than this – possibly as high as 10^5. The double spin filter tunnel junction (DSFTJ) reverses the usual structure of spin devices in that the tunnel barrier material is formed from two different layers that are insulating but are magnetic and exhibit unequal coercivities Figure 9. The coercivity of one layer is chosen to be very large so that it remains "pinned" (unable to be changed), while the other has a smaller value that the direction of its magnetization can be changed more easily.
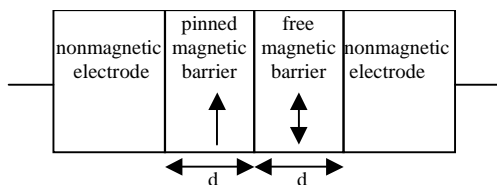

Figure 9 Double Spin Filter Junction (from **[31]**)

In DSFTJ layout proposed in Figure 10, the thin magnetic barriers are formed on the surface of a conductive pillar. The resistance is varied between the inner pillar and the multiple outer conductors that provide nearest neighbour connection. In this case a square lattice is shown but other layouts (e.g. hexagonal) would be equally possible.
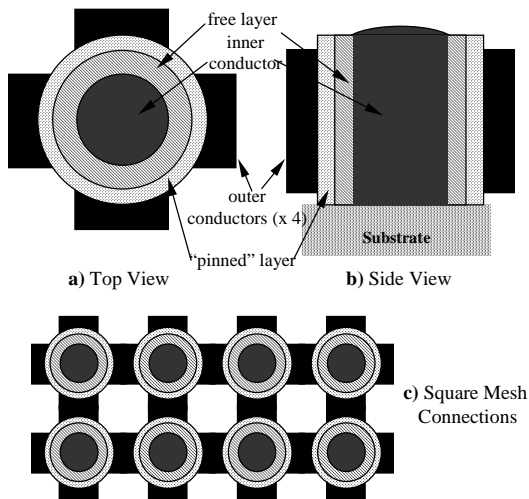

Figure 10 The "Bullseye" Double Tunnel Junction

While much of the enabling technology exists, there are still a number of significant technical challenges to be overcome to make the device work. High density pillars of metallic and/or magnetic materials have been grown for applications such as quantized magnetic disk technology. Techniques such as e-beam lithography, RIE and plating or nano-imprint lithography have resulted in the production of pillars and rings of material down to 10nm diameters on 40nm centers with aspect ratios of 10:1 [32]. However, it is likely to be difficult to find materials with just the right combinations of small band gap and large exchange splitting, that exhibit appropriate hysteresis curves and can be grown in thin, pinhole-free layers on a lattice-matched conductor. It has been demonstrated that ferrites can be grown epitaxially on $SrTiO_3$ [33] so this would represent a good starting point in the search for suitable materials.

The model for the DSFTJ developed by Worledge and Geballe [31] predicts that its magnetoresistance will be an exponential function of the layer thicknesses so the device becomes more sensitive as the thickness of the barrier layers is increased. Unfortunately, its resistance is also an exponential function of barrier thickness making it difficult to control the summing currents between devices[3]. The programming current must be able to be set at a value sufficient to saturate the free layer without switching the pinned layer which implies that either the two layers must start with widely differing coercivities, or the variation across the mesh needs to be very closely controlled.

A careful tradeoff will need to be made between the thickness (and therefore the GMR), the tunnel resistance, the coercivity of the two layers and the available programming current. Other important issues will include magnetostatic interactions not only between the layers but possibly between the adjacent nanomagnets within the array [34], the effect of diameter and thickness on the hysteresis curves [35] and domain duplication between layers [36].

The adjacent devices create a logic mesh in which resistive interconnections may be created by manipulating (programming) the magnetic fields within the spin junctions. In the network of Figure 11, currents are summed into the non-linearity of the RTD. This logic array is functionally identical to the collection of resistively coupled quantum dots proposed by Roychowdhury et al [37] except that now the connectivity is programmable and non-volatile. Just as in Roychowdhury's proposal, achieving uni-directional logic operation is a potential problem with this array.

Processing would start with the RTD substrate followed by the patterning of the top RTD contacts. The contacts would then form both the mask for the mesa etch stage of the RTD and the seed points for

---

[3] For the example given in [31], a 1% change in *d* will result in a 13% change in resistance.

the growth of the contact pillars. Finally, after epitaxial deposition of the magnetic layers over the pillars and patterning the interconnect metal, a layer of oxide would be grown and planarized ready to take the upper layer of active devices.

A straightforward way to address and program the individual junctions is to arrange them in a RAM-like array by integrating an isolation transistor into the cell (Figure 11). A Vertical Tunnelling Transistor (VTT) [38] would be particularly suited to this application as it can be formed by a selectively patterned epitaxial metallisation of a SOI substrate grown over the magnetic array and the overall device is likely to be scalable to less than 1nm square, while maintaining high current density.
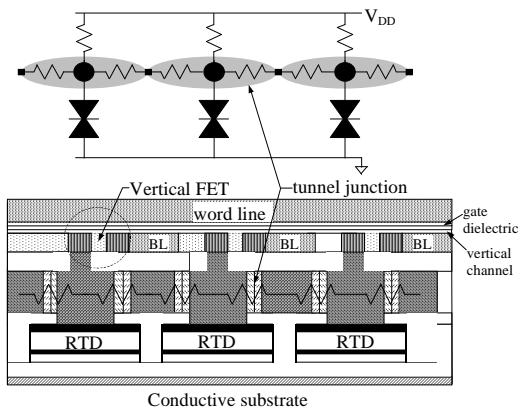

Figure 11 Magnetic Logic Element

In this case, the VTT is connected, via the lower side of its source, to the central pillar of the DSFTJ and acts both to supply the programming currents and to read the voltage level of the result. The top side of the source is pulled up to V_{DD} via a thin-film resistor or similar (not shown). Only one current pulse[4] is needed to configure devices to on or off. In additional, the isolation transistor provides a convenient way of applying a global signal (such as a multiphase clock signal) to the logic mesh.

This vertically integrated approach could eventually support tunnel junction densities in excess of $2 \times 10^{11}/cm^2$, although how this translates into logic gates is complicated by a number of issues. Firstly, while it takes a minimum of three junctions to form a two-input logic gate, each independent logic

block must be surrounded by a palisade of isolation cells. The actual number of these isolation cells will depend the logic optimisation and the actual placement topology and has an optimistic lower bound of $4mn^{1/2}$ (for m logic blocks each with n junctions) - which tends to favour fewer, larger blocks as a layout strategy. Isolation also needs to be provided for faulty gates. This includes not only hard failures (i.e. short-circuits) but devices that fail logic and/or parametric tests – exhibiting low current or longer than acceptable delay times. While it is clear that reconfiguration is a very powerful technique for maintaining reliability in a logic network [39], most analyses appear to be based on the assumption that faults are randomly distributed and their effects are localised. However, the blocking caused by a cluster of faults in an area may cause significant "flow-on" effects for that could conceivably cause a large number of otherwise good cells to become unavailable to the place and route process.

As logical inversion is not possible in this type of system, all logic variables and their inverse must be maintained right through the system, potentially doubling the number of junction cells used for a particular function. Finally, as for standard MRAM devices, on-chip space is required by support circuits such as current-drive and voltage detection, address generation etc.

5 Reconfigurable Spatial Computing

The decision about how to perform a particular computational task has traditionally involved striking a balance between hardware and software – between the spatial and the temporal domains [40]. At one extreme, full custom hardware offers parallel spatial execution with very little flexibility or generality. At the other, software implementations exploit a more-or-less "general-purpose" platform to provide a flexible but lower performance solution.

To reduce the performance gap between these two extremes, complex hierarchical memory schemes have emerged that try to hide the cost of moving code and data items from one place to another in a processor system. However, it is clear that the returns from the increasingly complex structures used for functions such as speculation, reordering, and caching are rapidly diminishing (e.g. [41]) and may eventually become counter productive[5]. The move to nanoscale devices will accelerate this trend.

The concept of 3D memory has been proposed [43] as a way of bringing memory and processing

---

[4] this assumes that the "pinned" layer is set in manufacture and only the free layer is controllable. Relaxing this constraint offers some interesting extensions to the basic idea. The double tunnel junction is inherently a four-state device and the RTD has symmetrical characteristics about zero. Thus the cell intrinsically supports a balanced ternary logic representation that could be exploited to reduce logic complexity.

[5] Kozyrakis et al put it more strongly: *"cache memory is just a redundant copy of information that would not be necessary if main memory had kept up with processor speed"* [42].

physically closer together (Figure 12a). If the overheads associated with reconfigurability can be reduced sufficiently, there is no fundamental obstacle to completely removing this separation of memory and processing and with it the performance gap between the two. This may ultimately lead to a computing system in which all storage – registers, caches, main memory and even eventually disk – is unified within the processing mesh (Figure 12b).
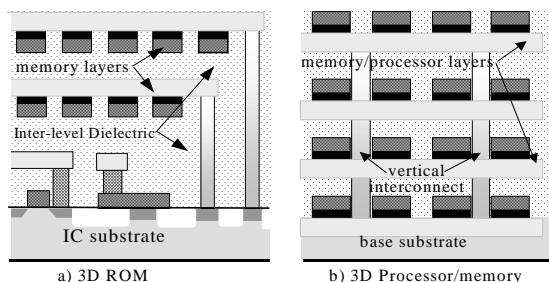

| a) 3D ROM | b) 3D Processor/memory |

Figure 12 Comparison between the 3D-ROM concept (from [43]) and 3D merged processor/memory.

6 Conclusions

In this paper, some ideas have been presented about how low-overhead reconfigurable systems might be built to exploit the characteristics of emerging nanoscale devices. Although not all of the enabling technology is currently available, the example circuits presented have demonstrated that it will be possible to exploit a number of alternative "dimensions" – apart from the obvious spatial dimension - to construct compact reconfigurable cells.

Dual-gate transistors are of great interest as they offer a way of avoiding short channel effects and substrate leakage (in CMOS) as channel length is scaled down. Given that the second gate can be justified on these grounds, the ability to configure the transistor's operating region can be added with very little additional overhead. All that is required is an efficient means of developing the multi-level reference voltages and this has been illustrated using both RTD and phase change chalcogenide devices.

A high-density non-volatile reconfigurable cell has been proposed in which a double junction spin filter tunnel junction is built on a vertical conducting pillar and integrated into a nearest neighbour-connected mesh. Whether the basic device can actually be built relies on the discovery of materials with the right combinations of small band gap and large exchange splitting, that exhibit appropriate hysteresis curves and can be grown in thin, pinhole-free layers on a lattice-matched conductor. The availability of this sort of high-density non-volatile reconfigurable mesh

can provide a flexible, defect tolerant platform that will allow novel 3D spatial computer architectures to be explored.

7 References

[1] Zhang, H., Prabhu, V., George, V., Wan, M., Benes, M., Abnous, A., Rabaey, J.M. *A 1 V Heterogeneous Reconfigurable Processor IC for Baseband Wireless Applications* in IEEE International Solid-State Circuits Conference, ISSCC 2000. 2000. pp. 68 -69, 448.

[2] Takahara, A., Miyazaki, T., Murooka, T., Katayama, M., Hayashi, K., Tsutsui, A., Ichimori, T., Fukami, K-n. *More Wires and Fewer LUTs: A Design Methodology for FPGAs* in ACM/SIGDA Sixth International Symposium on Field programmable Gate Arrays. 1998. pp. 12 - 19.

[3] de Dinechin, F., *The Price of Routing in FPGAs*. 1999, INRIA. Accessed: 26 September, http://citeseer.nj.nec.com/dedinechin99price.html

[4] Hauck, S. *The Future of Reconfigurable Systems* in 5th Canadian Conference on Field Programmable Devices. 1998.

[5] Endoh, T., Suzuki, M., Sakuraba, H., Masuoka, F., *2.4F^2 Memory Cell Technology with Stacked-surrounding Gate Transistor (S-SGT) DRAM.* IEEE Transactions on Electron Devices, 2001. **48**(8): 1599 - 1603.

[6] Endoh, T., Sakuraba, H., Shinmei, K., Masuoka, F. *New Three Dimensional (3D) Memory Array Architecture for Future Ultra High Density DRAM* in 22nd International Conference on Microelectronics. 2000. pp. 447 -450 vol.2.

[7] Wei, S.-J., Lin, H.C., *Multivalued SRAM Cell Using Resonant Tunneling Diodes.* IEEE Journal of Solid-State Circuits, 1992. **27**(2): 212-216.

[8] van der Wagt, J.P.A., *Tunnelling-Based SRAM.* Nanotechnology, 1999. **10**(2): 174-186.

[9] Mathews, R.H., Sage, J.P., Sollner, T.C.L.G., Calawa, S.D., Chang-Lee Chen, Mahoney, L.J., Maki, P.A., Molvar, K.M., *A New RTD-FET Logic Family.* Proceedings of the IEEE, 1999. **87**(4): 596 - 605.

[10] Fukushima, K., Sasajima, R., Fujimaru K., Matsumura, H., *A Novel Nanoscale Metal Transistor Fabricated by Conventional Photolithography.* Japanese Journal Applied Physics, 1999. **38 Part 1**(12B): 7233-7236.

[11] Snow, E.S., Campbell, P. M., Rendell, R. W., Buot, F. A., Park, D., Marrian, C. R. K., Magno, R., *A Metal/Oxide Tunneling Transistor.* Applied Physics Letters, 1998. **72**(23): 3071-3073.

[12] Zhang, R., Roy, K., Janes, D. B. *Architecture and Performance of 3-Dimensional SOI Circuits* in 1999 IEEE International SOI Conference. 1999. pp. 44-45.

[13] Saraswat, K.C., Souri, S.J., Subramanian, V., Joshi, A.R., Wang, A.W. *Novel 3-D structures [ICs]* in 1999 IEEE International SOI Conference. 1999. pp. 54 -55.

[14] Chan, V.W.C., Chan, P. C. H., Chan, M., *Multiple Layers of CMOS Integrated Circuits Using*

Recrystallized Silicon Film. IEEE Electron Device Letters, 2001. **22**(2): 77-79.

[15] Rakitin, V.V., Filippov, E.I., *Logical Elements Based on Dual MOS Transistors.* 1996. Accessed: 24/12/01, http://www.niifp.ru/english/nano/lebdmos.html

[16] Chang, L., Tang, S., Tsu-Jae King, Bokor, J., Chenming Hu. *Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs* in International Electron Devices Meeting. 2000. pp. 719 - 722.

[17] Collier, N.J., Cleaver, J. R. A., *Novel Dual-Gate HEMT Utilising Multiple Split Gates.* Microelectronic Engineering, 1998. **41-42**: 457-460.

[18] Suehiro, H., Miyata, T., Hara, N., Kuroda, S., *A 48.1 ps HEMT DCFL NAND Circuit with a Dual Gate Structure.* Solid-State Electronics, 1995. **38**(9): 1717-1721.

[19] Seabaugh, A.C., Kao, Y.-C., Yuan, H.-T., *Nine-state Resonant Tunneling Diode Memory.* IEEE Electron Device Letters, 1992. **13**(9): 479 -481.

[20] Compano, R., (ed.) *Technology Roadmap for Nanoelectronics.* 2nd ed, in. 2000, European Commission IST Programme - Future and Emerging Technologies.

[21] Nakayama, K., Kojima, K., Hayakawa, F., Imai, Y., Kitagawa, A., Suzuki,M., *Submicron Nonvolatile Memory Cell Based on Reversible Phase Transition in Chalcogenide Glasses.* Japanese Journal Applied Physics, 2000. **39**(Part 1, No. 11): 6157-6161.

[22] Gill, M., Lowrey, T., Park, J. *Ovonic Memory - A High Performance Non-Volatile memory Technology for Stand-Alone Memory and Embedded Applications* in to be published in IEEE International Solid-State Circuits Conference. 2002.

[23] Tyson, S., Wicker, G., Lowrey, T., Hudgens, S., Hunt, K. *Nonvolatile, High Density, High Performance Phase-Change Memory* in IEEE Aerospace Conference. 2000. pp. 385 -390 vol.5.

[24] Lowrey, T., *Ovonic Unified Memory.* 2001, Ovonyx Pty. Ltd., Troy, Michigan, U.S.A.

[25] Sylvester, D., Keutzer, K., *A Global Wiring Paradigm for Deep Submicron Design.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2000. **19**(2): 242 -252.

[26] Johnson, M., *Magnetoelectronic Memories Last and Last...* IEEE Spectrum, 2000. **37**(2): 33 -40.

[27] Cowburn, R.P., Welland, M. E., *Room Temperature Magnetic Quantum Cellular Automata.* Science, 2000. **287**: 1466 - 1468.

[28] Katti, R.R., Zhu, T., *Attractive Magnetic Memories.* IEEE Circuits and Devices Magazine, 2001. **17**(2): 26 -34.

[29] Tang, D.D., Wang, P.K., Speriosu, V.S., Le, S., Kung, K.K., *Spin-valve RAM cell.* IEEE Transactions on Magnetics, 1995. **31**(6 Part: 1): 3206 -3208.

[30] Shen, J., *Logic Devices and Circuits based on Giant Magnetoresistance.* IEEE Transactions on Magnetics, 1997. **33**(6): 4492 - 4497.

[31] Worledge, D.C., Geballe, T. H., *Magnetoresistive Double Spin Filter Tunnel Junction.* Journal of Applied Physics, 2000. **88**(9): 5277-5279.

[32] Chou, S.Y., Patterned Magnetic Nanostructures and Quantized Magnetic Disks. Proceedings of the IEEE, 1997. **85**(4).

[33] Suzuki, M.I., K., Ida, T., Aoyagi, Y., *Quantum Dot Formation in Single-Wall Carbon Nanotubes.* Japanese Journal Applied Physics, 2001. **40, Part 1**(3B): 1915-1917.

[34] Cowburn, R.P., Adeyeye, A. O., Welland, M. E., *Controlling Magnetic Ordering in Coupled Nanomagnet Arrays.* New Journal of Physics, 1999. **1**(16): 16.1–16.9.

[35] Dao, N., Whittenburg, S. L., Cowburn, R. P., *Micromagnetics Simulation of Deep-Submicron Supermalloy Disks.* Journal of Applied Physics, 2001. **90**(10): 5235-5237.

[36] Lacour, D., Hehn, M., Lenoble, O., Schuhl A., Tiusan, C., Ounadjela, K., *Domain Duplication in Ferromagnetic Sandwiches.* Journal of Applied Physics, 2001. **89**(12): 8006-8010.

[37] Roychowdhury, V.P., Janes, D.B., Bandyopadhyay, S., *Nanoelectronic Architecture for Boolean Logic.* Proceedings of the IEEE, 1997. **85**(4): 574 -588.

[38] Tucker, J.R., Wang, C., Shen, T.-C. *A Nanoscale Vertical-Tunneling FET* in 53rd Annual Device Research Conference. 1995. pp. 24 - 25.

[39] Nikolic, K., Sadek, A., Forshaw, M., *Architectures for Reliable Computing with Unreliable Nanodevices.* 1st IEEE Conference on Nanotechnology, IEEE-NANO 2001, 2001: 254 -259.

[40] DeHon, A., *Trends Toward Spatial Computing Architectures.* IEEE International Solid-State Circuits Conference, ISSCC'99, 1999: 362 - 363.

[41] Bondalapati, K., Prasanna, V. K., *Reconfigurable Computing: Architectures, Models and Algorithms.* 2000. Accessed: 10/12/01, http://citeseer.nj.nec.com /295261.html

[42] Kozyrakis, C.E., Perissakis, S., Patterson, D., Anderson, T., Asanovic, K., Cardwell, N., Fromm, R., Golbus, J., Gribstad, B., Keeton, K., Thomas, R., Treuhaft, N., Yelick, K., *Scalable Processors in the Billion-Transistor Era: IRAM.* Computer, 1997. **30**(9): 75 -78.

[43] Zhang, G., *3D-ROM - A First Practical Step Towards 3D-IC.* 2000, Cahners Semiconductor International. Accessed: 12/01/02, http://209.67.253.149/semicon ductor/Issues/webexclusives/2000/200007/six00063D ROM.asp