Towards a Reconfigurable Nanocomputer Platform

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The Nanoscale "Cambrian Explosion"

- Disparity:
  - Wide range of emerging non-Si technologies
- Diversity:
  - Many new device options in CMOS, GaAs and other non-Si

Example Nanoscale Devices

Disparity →

← Diversity

Silicon	Hetero-junction	Nanotube	Molecular	Magnetic	Q-Well
SOI Si-Ge Dual-gate Vertical FET Ballistic nano-FET	RTD/ HFET RTT logic & memory Multi-valued logic nano-pipelining	CNT C60 logic & memory Nanotube array logic Large-bandgap devices (AlN, BN)	Rotaxane molecular x-bar CAEN Coulomb-coupled optically pumped nanodevices DNA	GMR/ CMR MQCA Hybrid-Hall effect Molecular nano-magnetics Magnetic RTD	Quantum dot Quantum diffraction FET Quantum interference devices surface super-lattices RSFQ

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The "Ideal" Nanocomputer Platform?

- Very large, scalable with rich, local connectivity
- Built from simple devices that exhibit:
  - **High functionality (?)**
  - **Gain > 1**
  - **Static (at least) and preferably non-volatile operation**
  - **(Very) low power density**
  - **Room temperature operation**
- Reliable and fault tolerant
- Preferably no intrinsic reliance on any form of global signal (e.g. a master clock)
- Reconfigurable in operation, with little or no performance penalty

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Three Example Nanoscale Systems

1. Multi-valued SRAM Based Platform
   - RTD multi-valued RAM
   - Dual-gate transistors
2. Phase Transition Device Based Platform
   - Resistive thin-films
3. A Nano-Magnetic Platform
   - Double spin-filter junction

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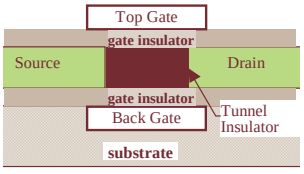
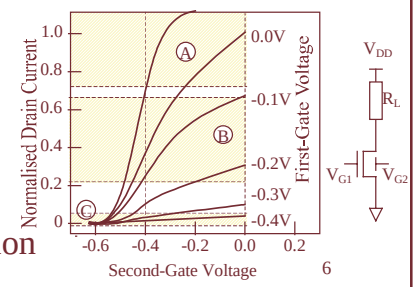
Multi-valued SRAM Based Platform

- metal-insulator tunnel transistor (MITT)
  - gate voltage modulates the tunnel barrier
- compatible with current fabrication processes
  - can be buried in oxide layer
- Proposed dual-gate increases functionality
  - Low-overhead reconfiguration





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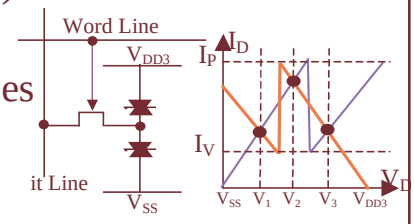
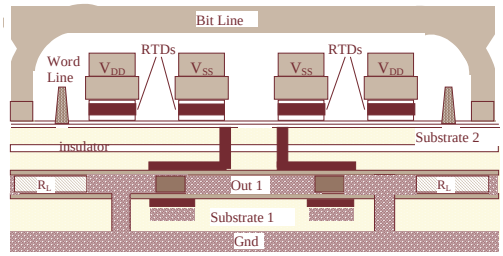
Multi-valued SRAM Based Platform

- 3-state memory (Wei & Lin)
- $V_{1\text{-}3}$ matched by adjusting RTD barrier layer thicknesses





- Ultimate dimensions 50nm
- ~3 x 10^9 cells/cm^2

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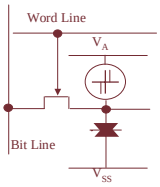
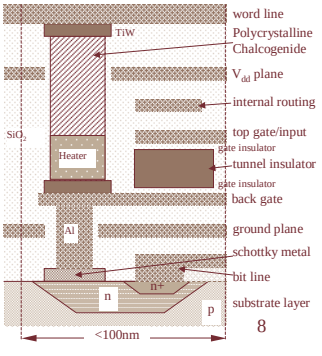
Non-volatility – Chalcogenide Films

- Chalcogenide films act as fast non-volatile programmable resistor
- Compatible with current (CMOS) logic fabrication
- Scales well to nanoscale dimensions (20-30nm)
- Vertical integration





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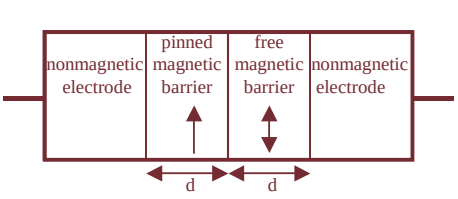
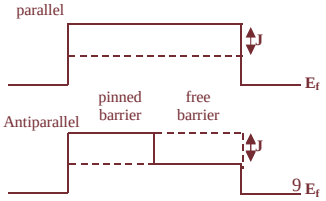
Double Spin-Filter Tunnel Junction

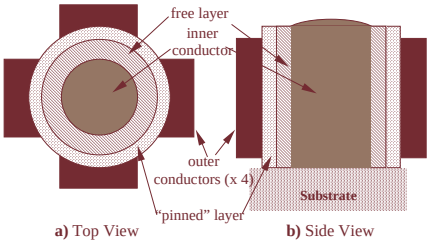
- Magnetoresistive tunnel device (Worledge & Geballe)
  - Potentially very high GMR
  - Formed from two different layers that are insulating but magnetic with unequal coercivities

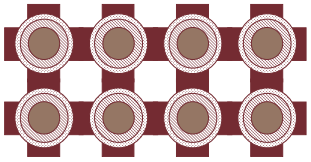




Vertical Double Spin-Filter Junction

- Resistance is varied between the inner pillar and the multiple outer conductors
- Requires ~20Å films on vertical pillar
  - No obvious candidates
- Thickness control and lattice matching will be important





c) Square Mesh Connections

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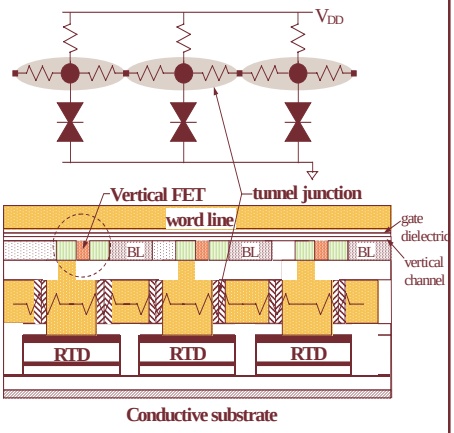
Spin-Filter Based Platform

- RTD substrate adds non-linearity to effect logic
- VTT for isolation
- Junction densities in excess of 2 x $10^{11}/cm^2$ possible



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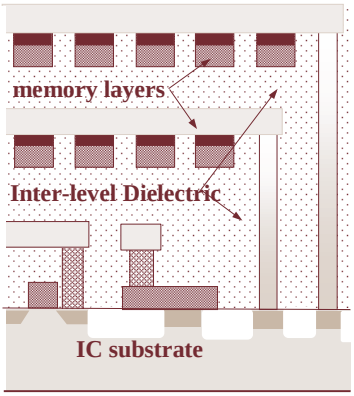
Spatial Computing

- Memory Hierarchy
  - Tries to hide the cost of moving code and data items from one place to another in a processor system
- 3D memory (Zhang)
  - Proposed as means memory and processing physically closer together



3D ROM

Zhang, 2000

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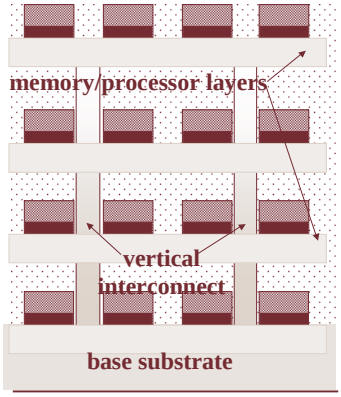
A 3D Reconfigurable Computing Platform

- Merged processor/ memory into 3D structure
- Reduced memory performance gap
- Extreme memory bandwidth
- Processing-in-memory; processing-is-memory



3D Processor/memory

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Reconfigurable Nanoelectronic Devices?

PRO

- Maximizes utility of small devices
- Reconfiguration over-heads kept small
- (Mostly) evolving from existing techniques
- Compatible with logic synthesis systems

CON

- Can they be built?
- Is the added complexity justified vs. (say) molecular approach?
- Will they efficiently support high-performance computer architectures

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What's Next?

- Simulation of nano-magnetic materials
- Characterization of typical junctions
  - e.g. tunneling conductance
- Simulation of GMR-based array platform
- Development of Spatial Computing techniques suited to this platform

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And in the long term?

- "Decimation followed by diversification" (Gould)
- Test against the "environment"
  - ease of fabrication, cost, ease of use etc.
- Extinction for some, consolidation and growth for others

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Thank You

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