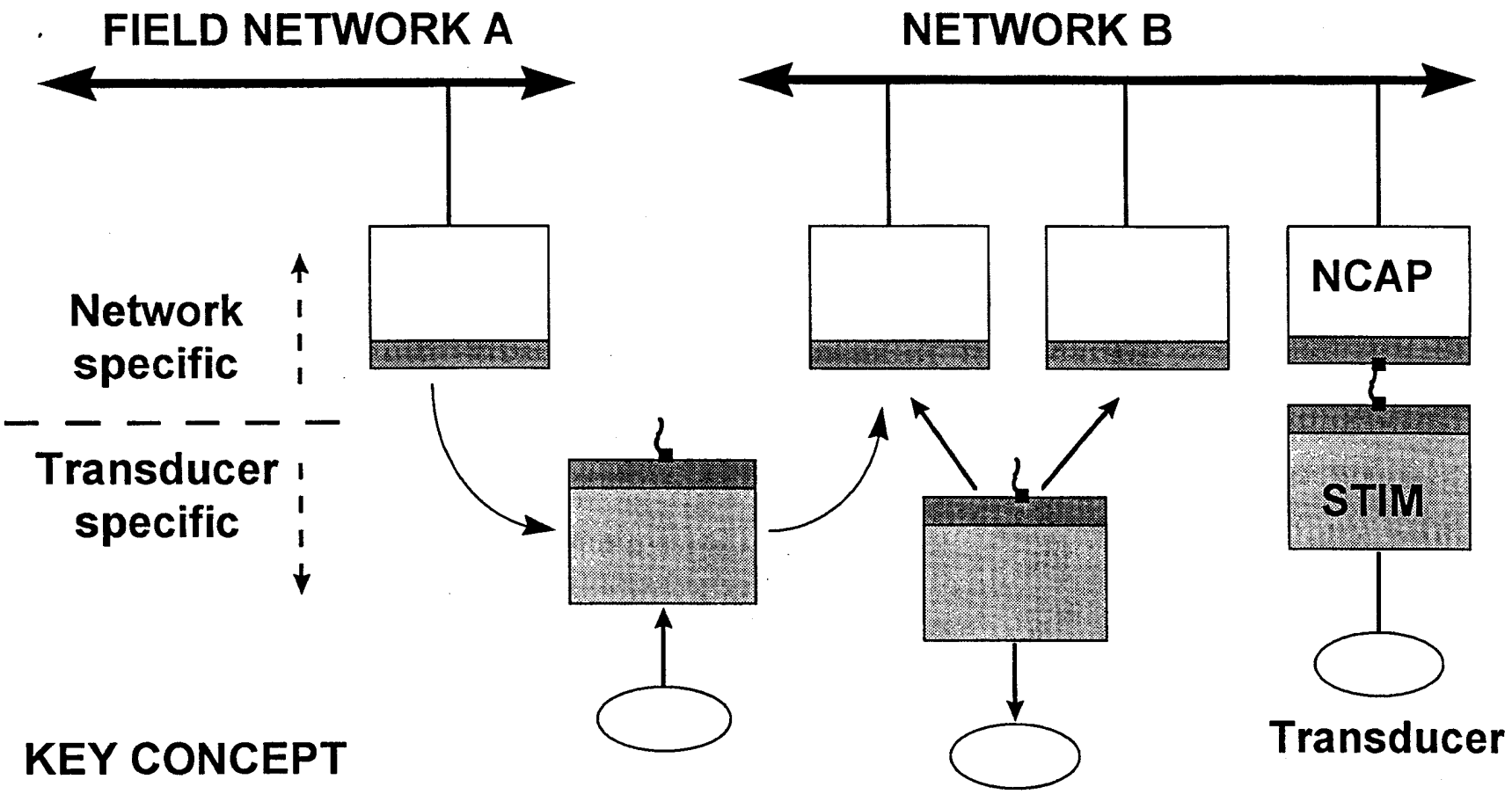
Outline

- Overview of IEEE 1451 Transducer Interface Std
- 12b Analog + EEPROM Integration Challenges
- Chip block diagram / photo
- 12b A-to-D converter:
- 12b DACs
- EEPROM cell
- On-chip downloader, debugger & emulator tools
- Conclusion

IEEE 1451.2 Transducer Interface Std



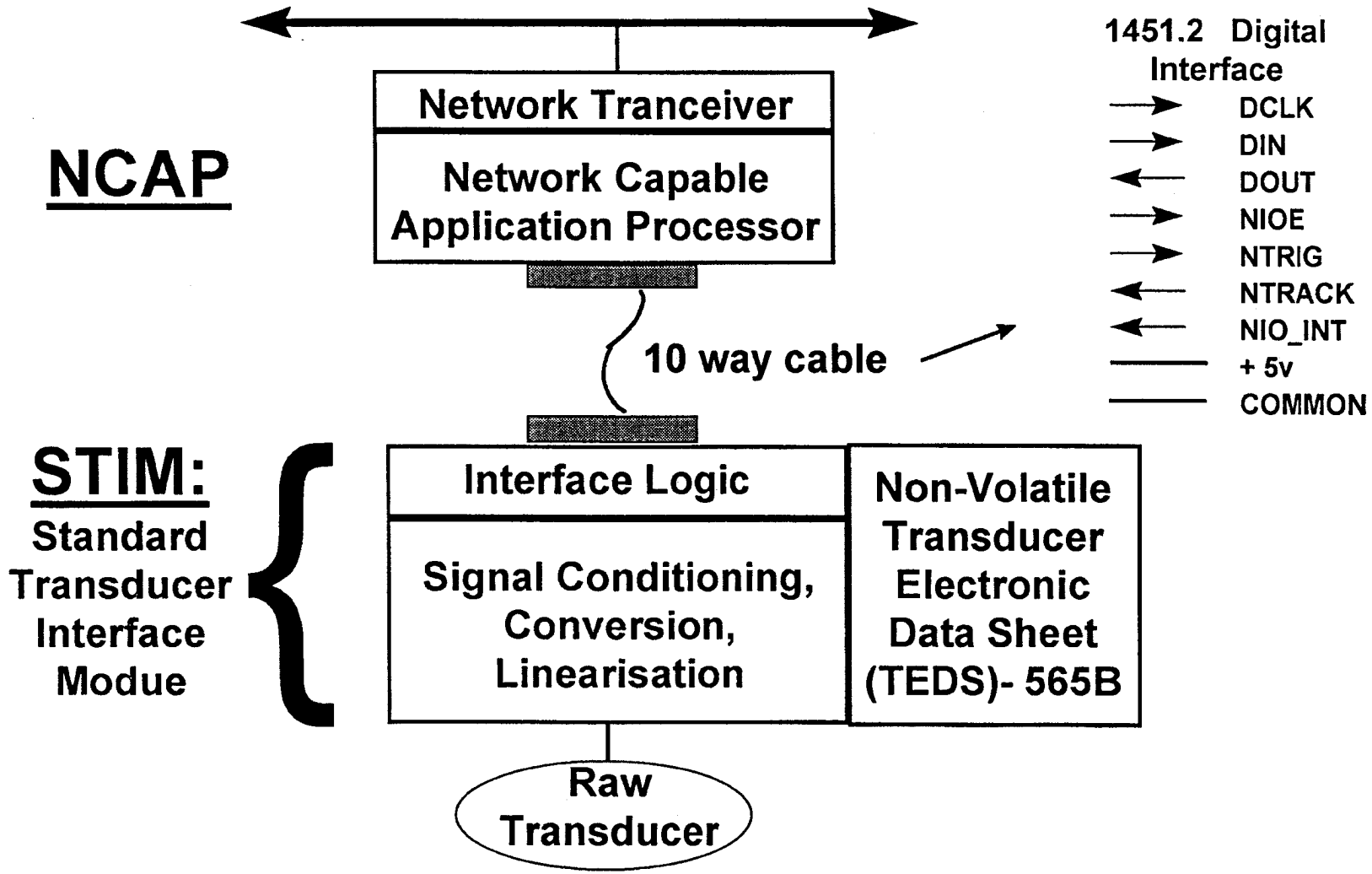
KEY CONCEPT

Transducers can be easily interchanged .....

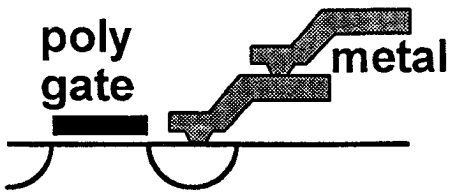
... between networks

... within networks

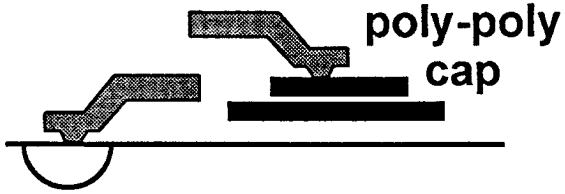
IEEE 1451.2 Std (contd)



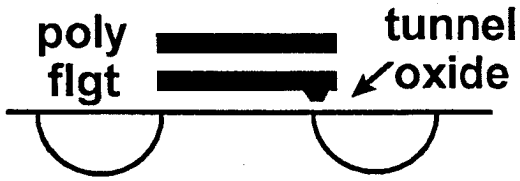
Analog+EEPROM Integration Challenges



CMOS: 12-13 masks



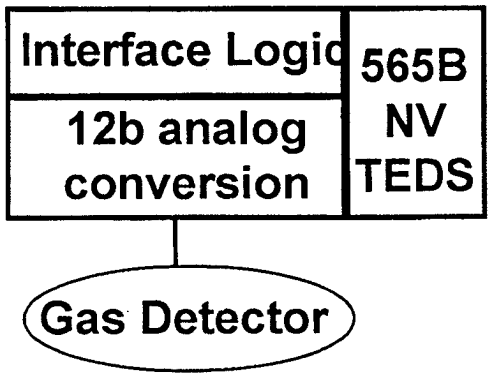
Mix-Sig CMOS: 14-16 masks



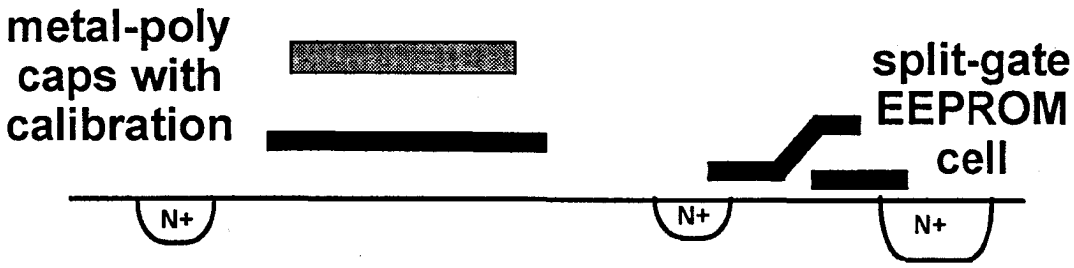
EEPROM: 19-21 masks

Traditionally v. difficult to integrate due to different process complexities

STIM:

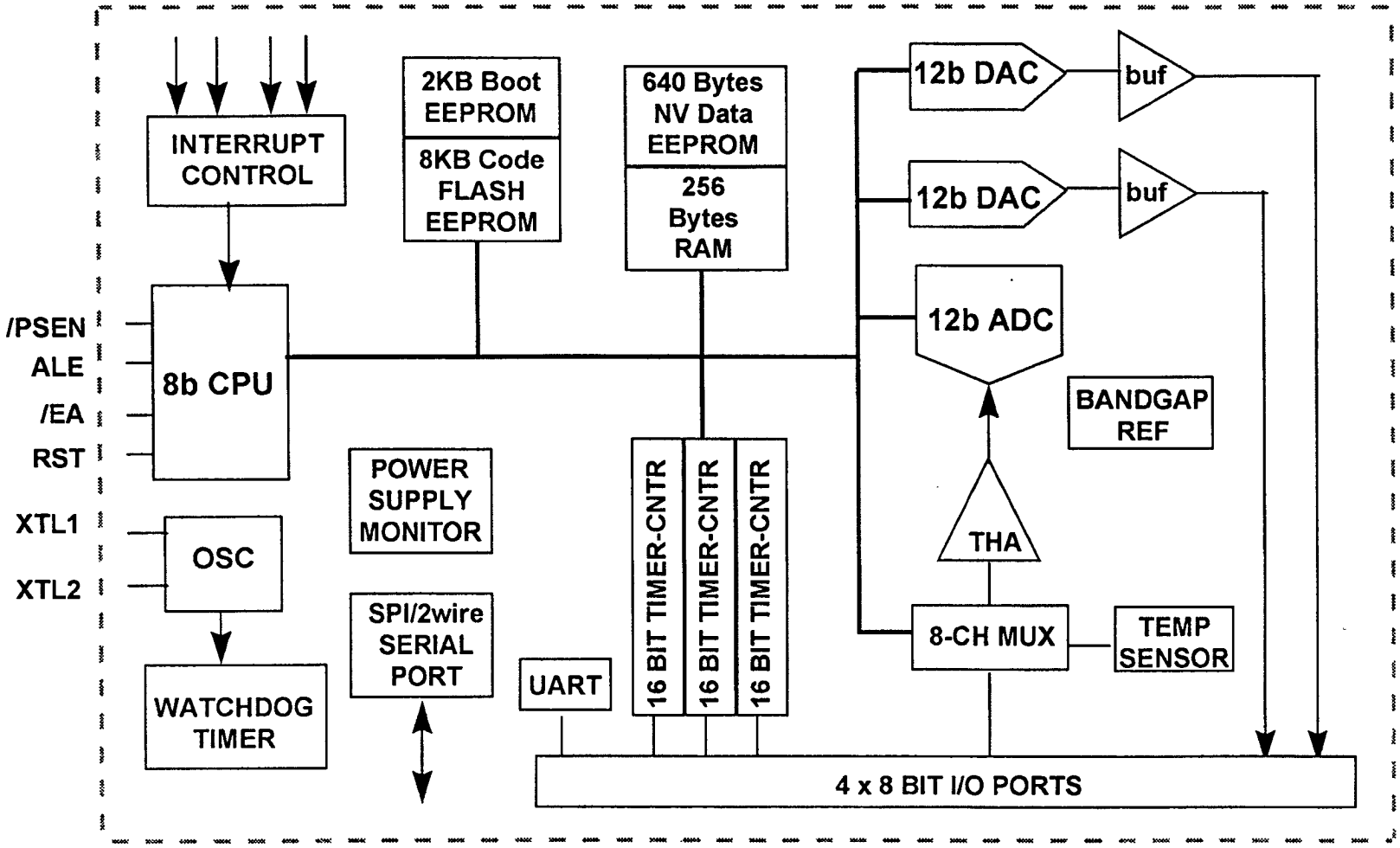


This chip:



CMOS with Emb split-gate Flash EEPROM: much simpler, only 15-18 masks

Chip Block Diagram

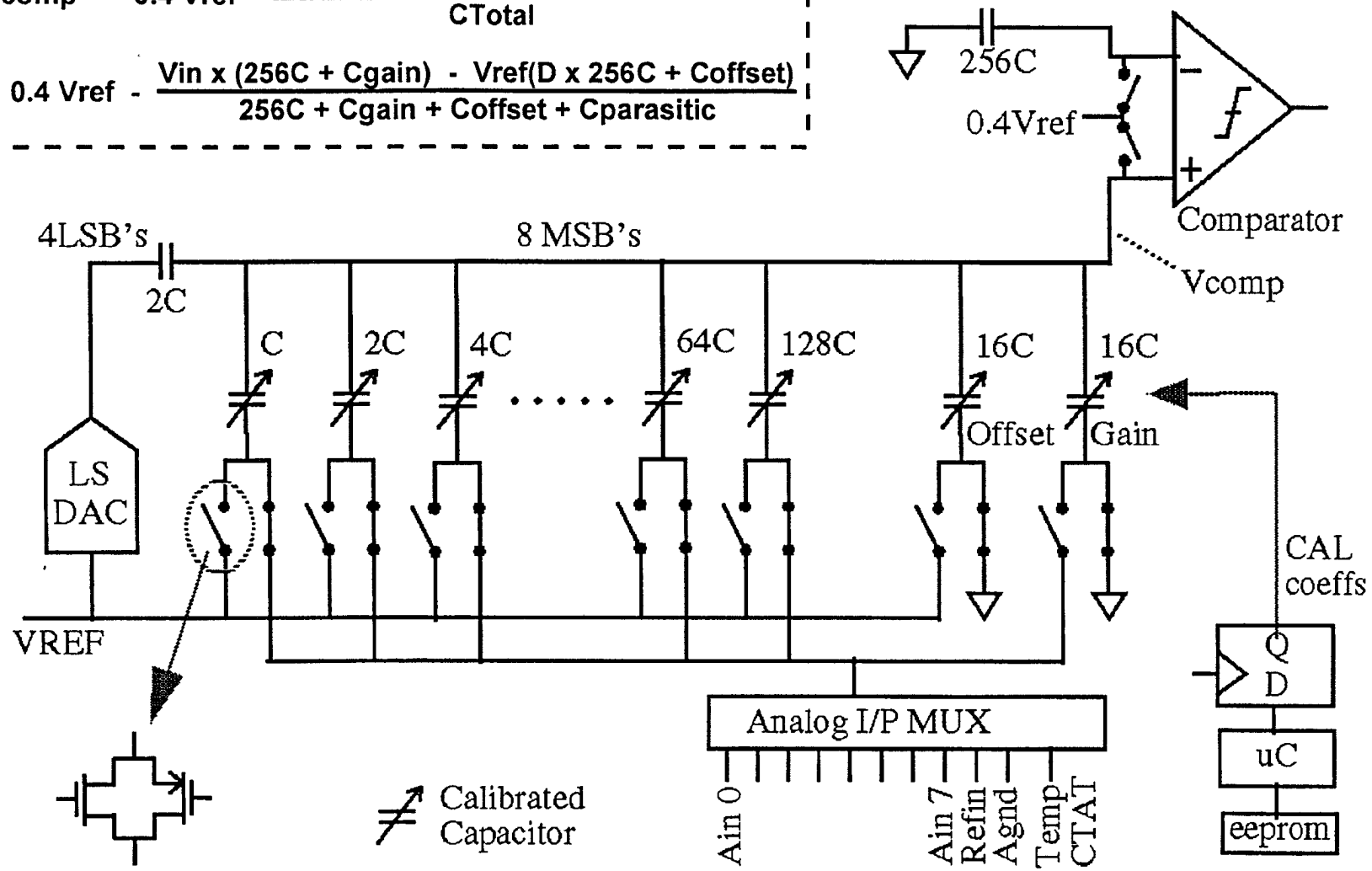


True 12-bit Analog Conversion + 8b uC + Flash EEPROM

8-ch 12b ADC - SAR DAC Schematic

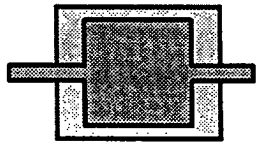
$$V_{comp} = 0.4\,V_{ref} - \frac{V_{in} \times C_{sample} - V_{ref} \times C_{dac} \times D}{C_{Total}}$$

$$= 0.4\,V_{ref} - \frac{V_{in} \times (256C + C_{gain}) - V_{ref}(D \times 256C + C_{offset})}{256C + C_{gain} + C_{offset} + C_{parasitic}}$$



12b Analog-to-Digital Converter

- SAR type, 8-channel, 12b, 5μs conversion
- Iaa = 1.5mA max
- Uses Metal-Poly capacitors with calibration to simplify process complexity;
- Unit Cap = 14 x 13 μm (7.64fF)



- Calibration coefficients:
  - Factory default values, or
  - in-situ per-channel values,
    e.g. transducer offset +/- 3% can be nulled

12b ADC - Performance & Results

DNL

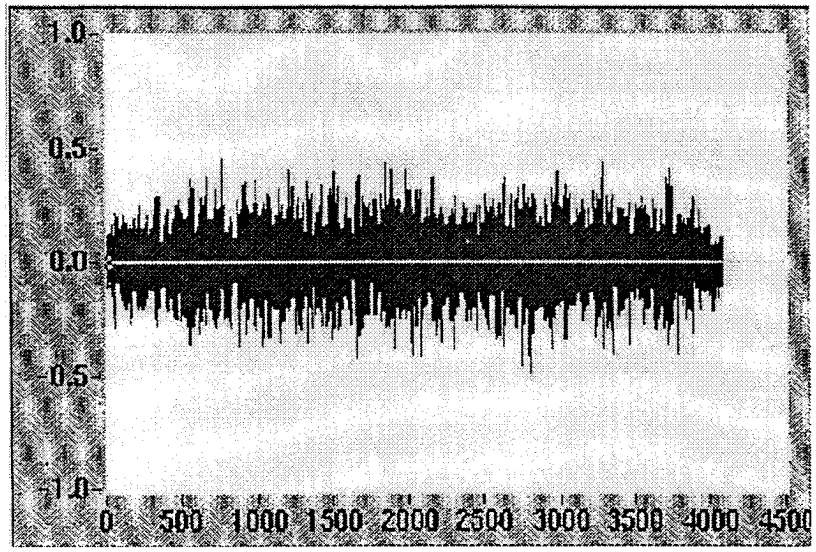
INL

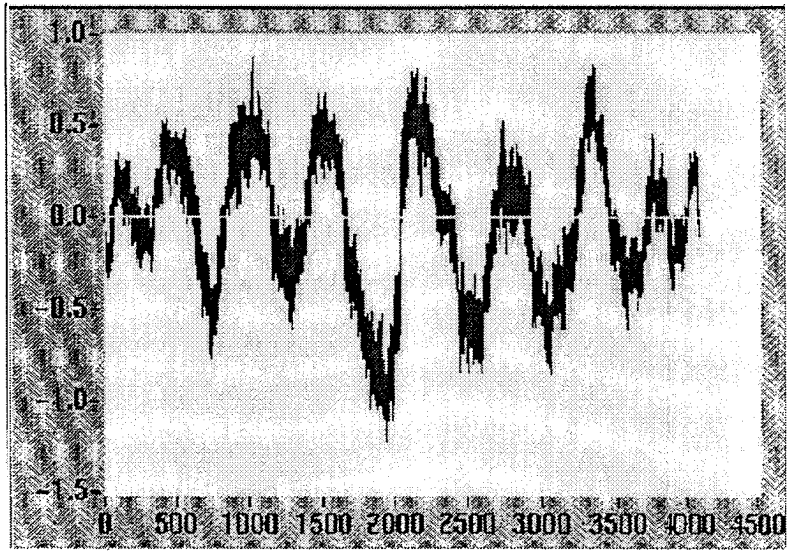
+1

0

-1

lsb

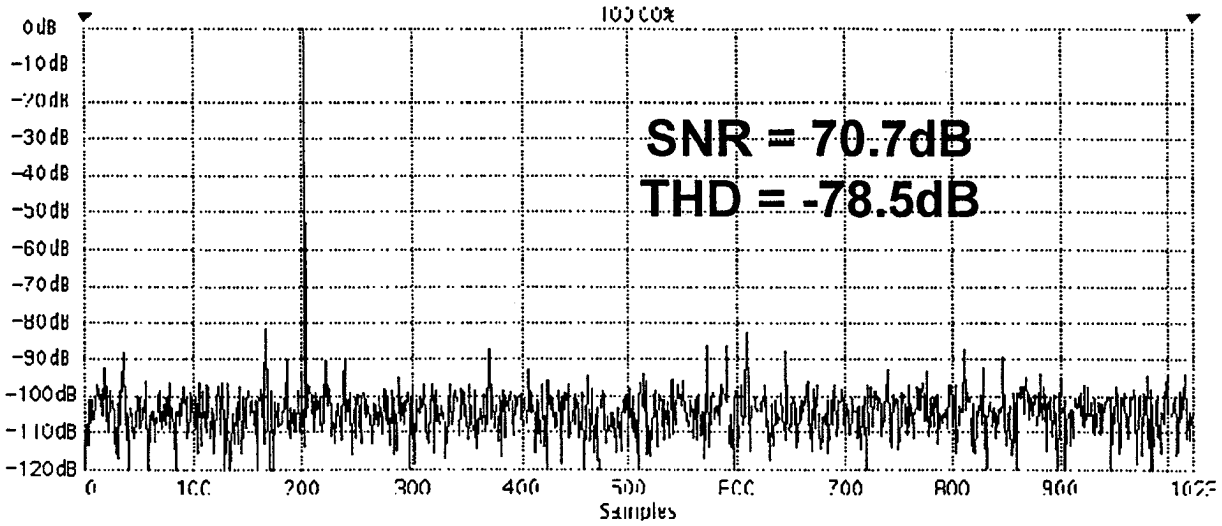




0 4095 0 4095

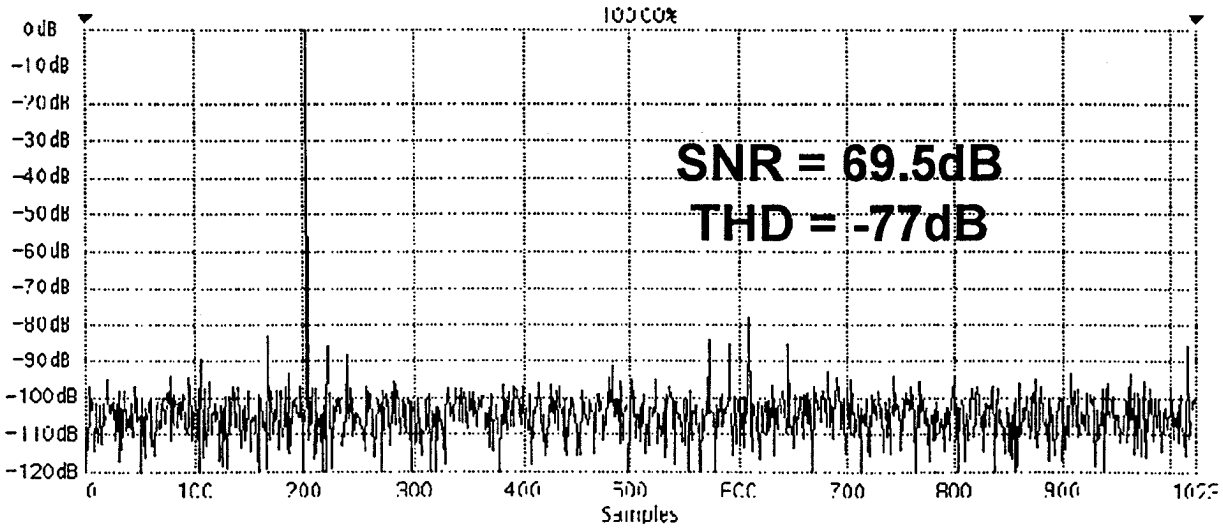
VCC = +3V
Vref = +2.5V
Fin = 1KHz
Temp = 25C

ADC SNR+THD



VCC = +5V
Vref = +5V
Fin = 2KHz
Fs = 25KHz
Temp = 25 C

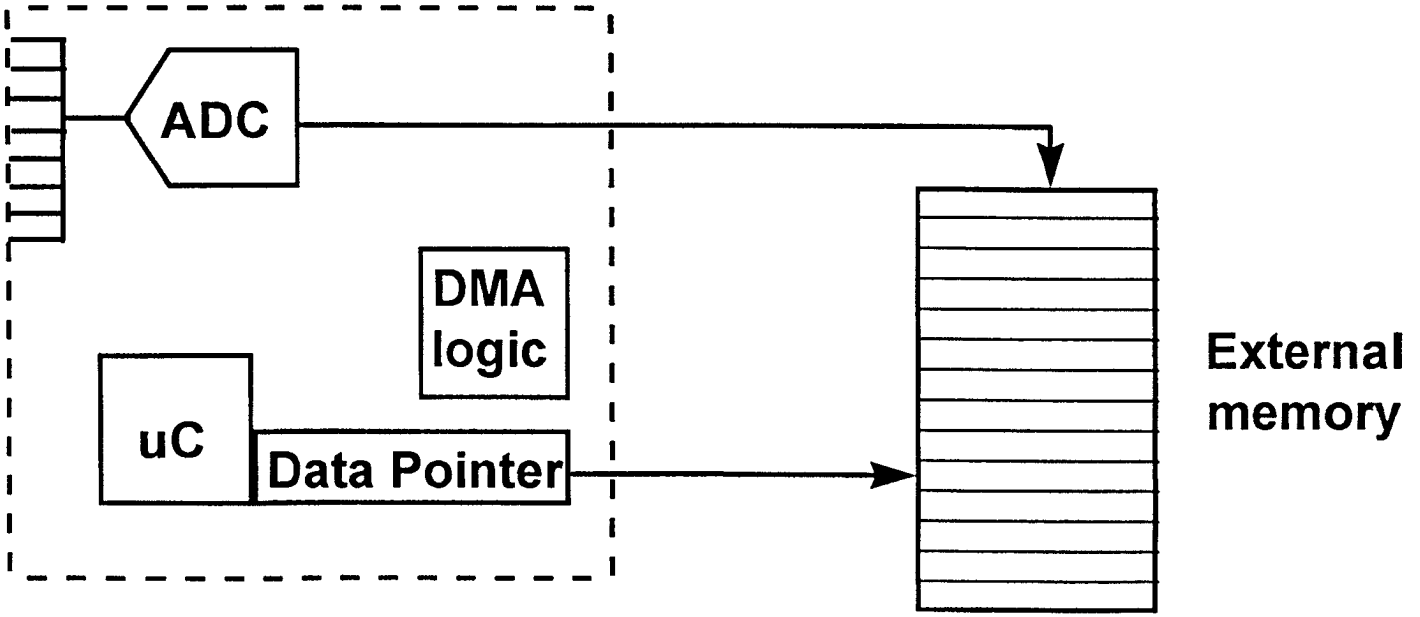
uC halted (ADC test mode)



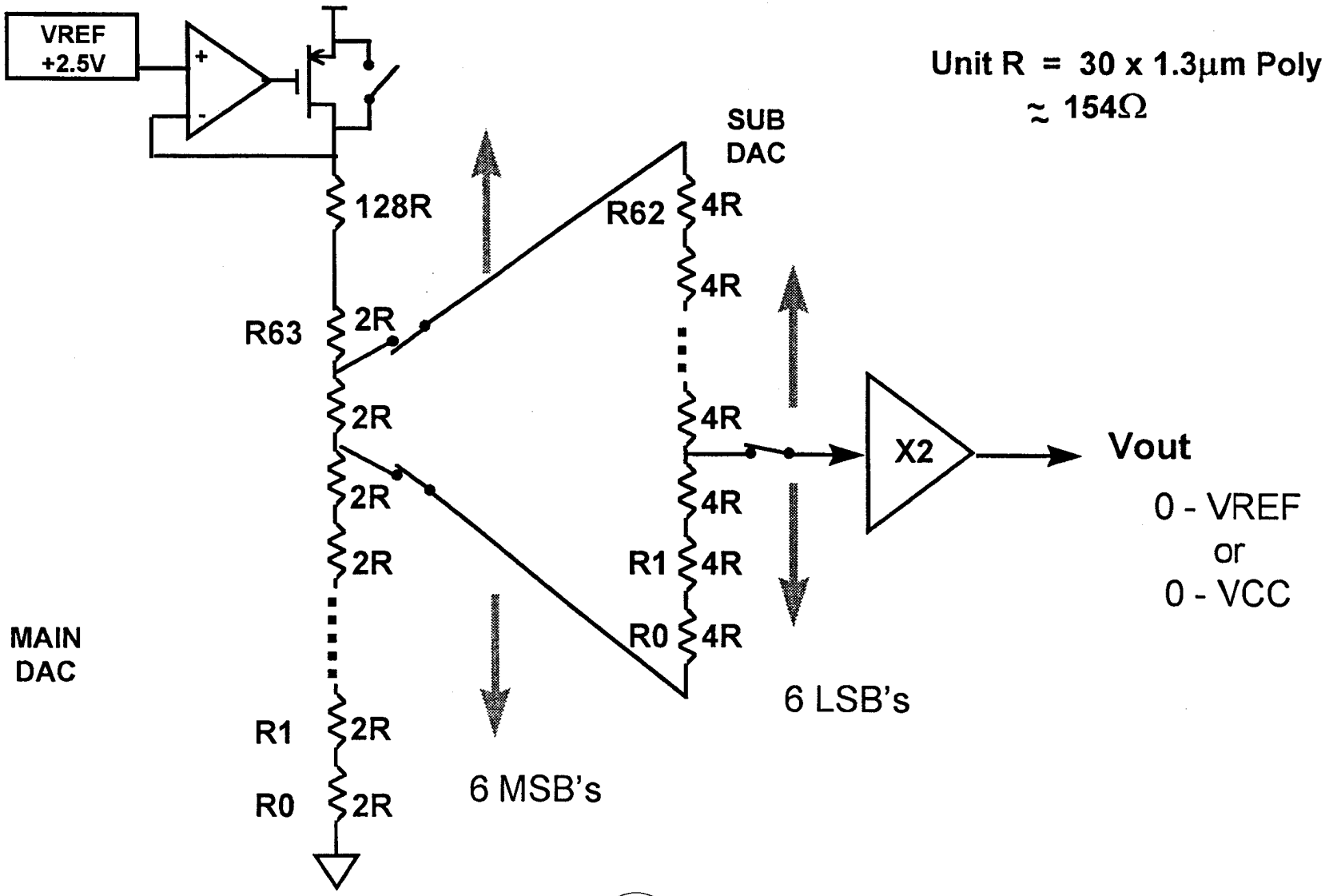
Code executing from internal EEPROM

ADC DMA Mode

- uC takes ~ 1uS per instruction @ Fclk 12MHz .... cannot service ADC at max conversion rate of 5μS/conv
- In DMA mode, ADC converts at max 5μs rate and stores results directly in external memory, e.g. for FFT analysis

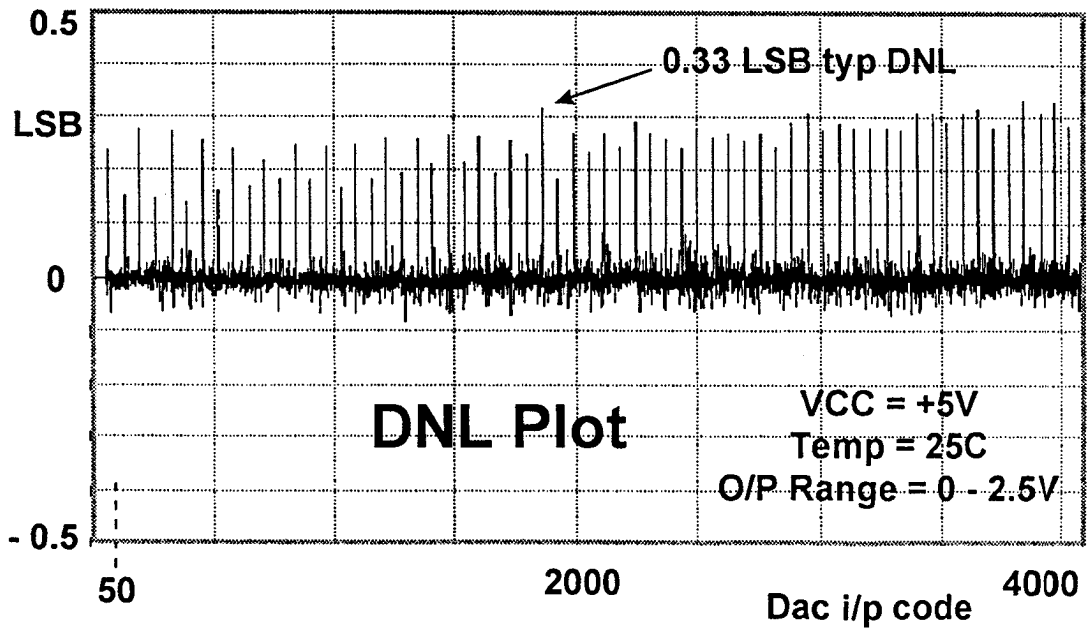


12b Digital-to-Analog Converter

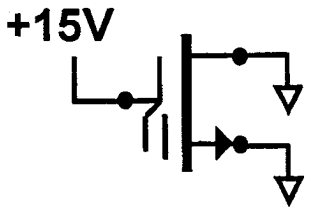


12b Digital-to-Analog Converter

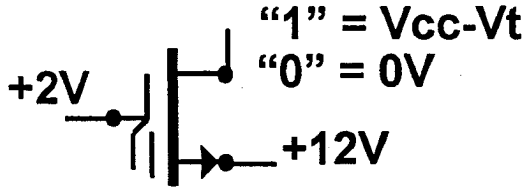
- Resistor string multiplying architecture, buffered Vout
- Two dacs on-chip: no need to use timers for PWM o/p
- Tconv = 10μs min (RL > 10KΩ, CL < 200pF)
- Iaa < 400uA
- DNL < 1 LSB



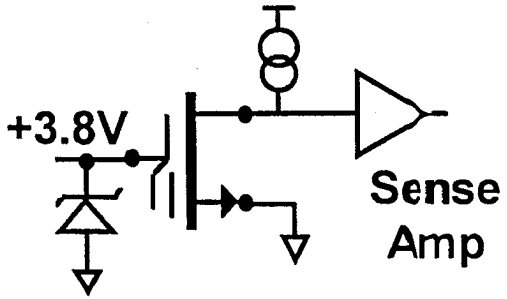
Split-Gate Flash EEPROM Cell



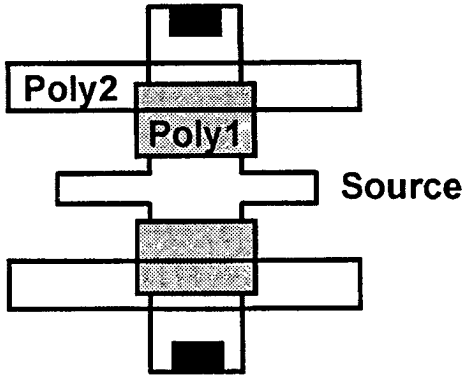
ERASE
Poly-Poly F-N Tunnelling



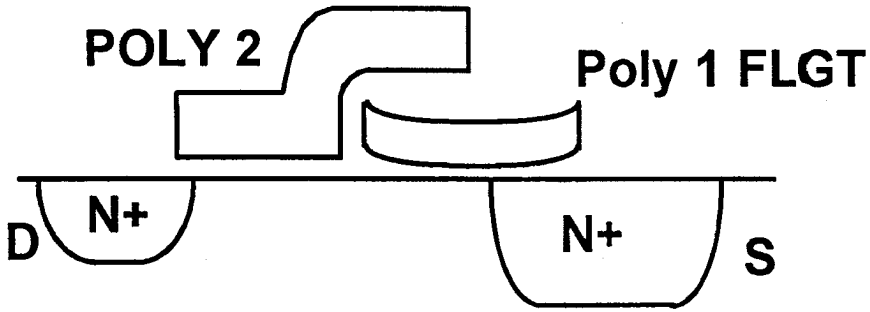
PROGRAM
CHE Injection



READ



Min Erase Sector is 2 rows



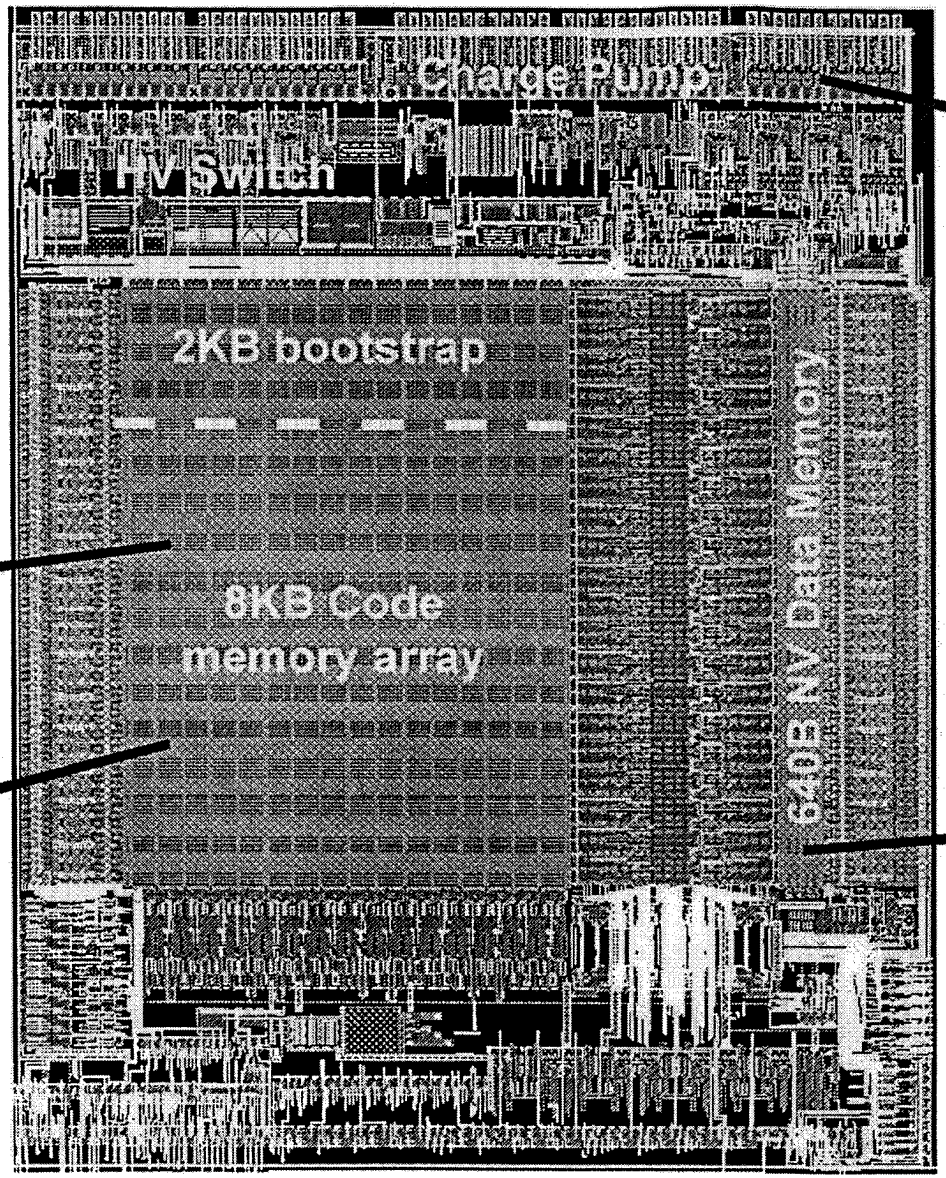
Prog & Erase are both Self-Limiting

EEPROM Block

Endurance
= 10K Cycles

Cell Size
= 4.7μm^2
(0.6μm rules)

Main Array =
320 row x 256 col
Min Erase sector:
2 rows (64 bytes)



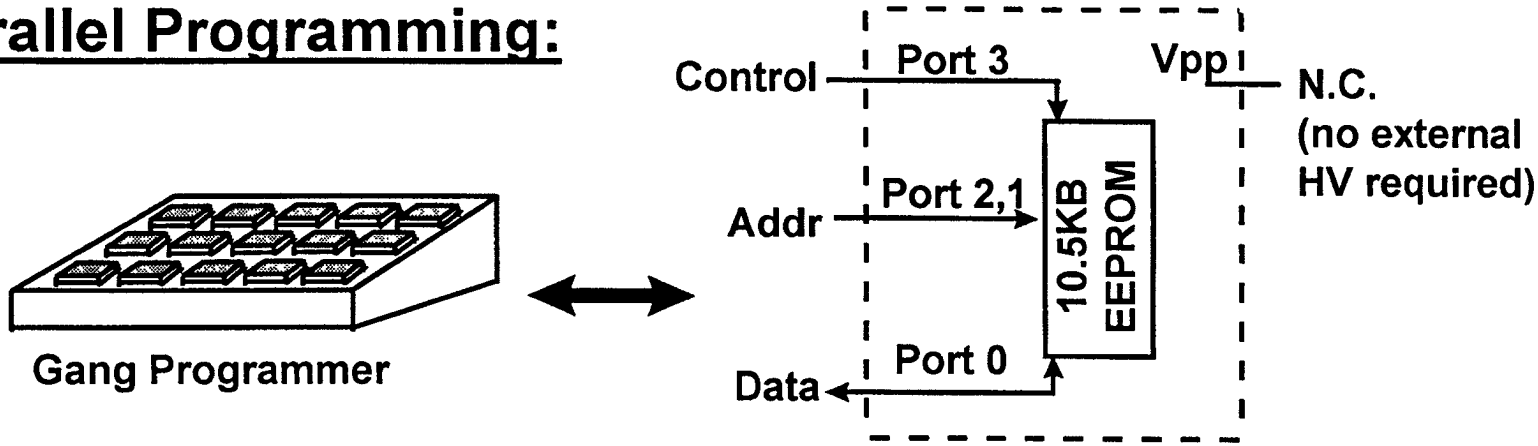
On-chip
charge pump:
no ext VPP
required.

Data Array =
320 row x 16 col
Min Erase secto
2 rows (4 bytes)

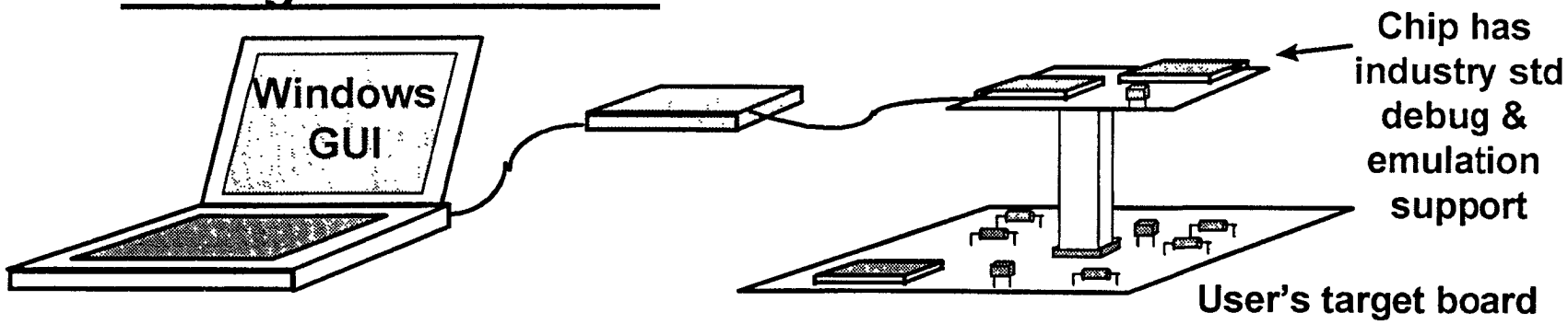
Software Support - I

- Chip supports industry standard 3rd party tools:

Parallel Programming:



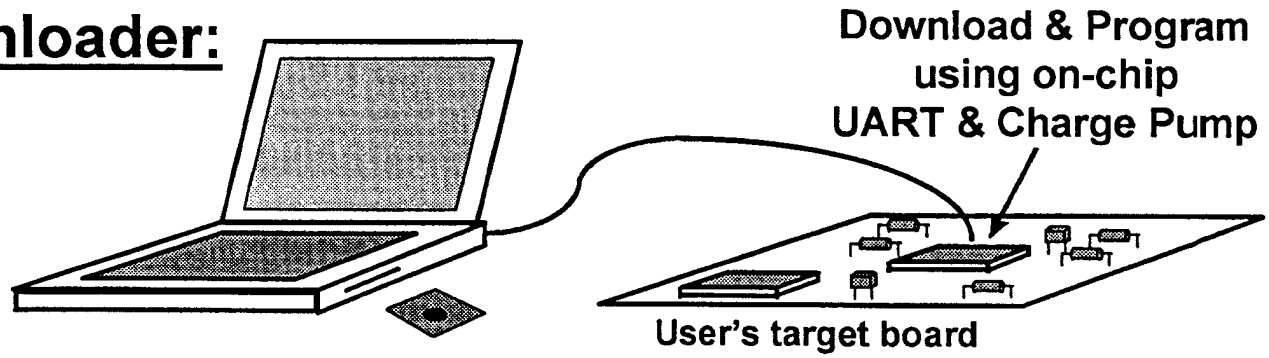
Debug & Emulation:



Software Support II - extra on-chip tools

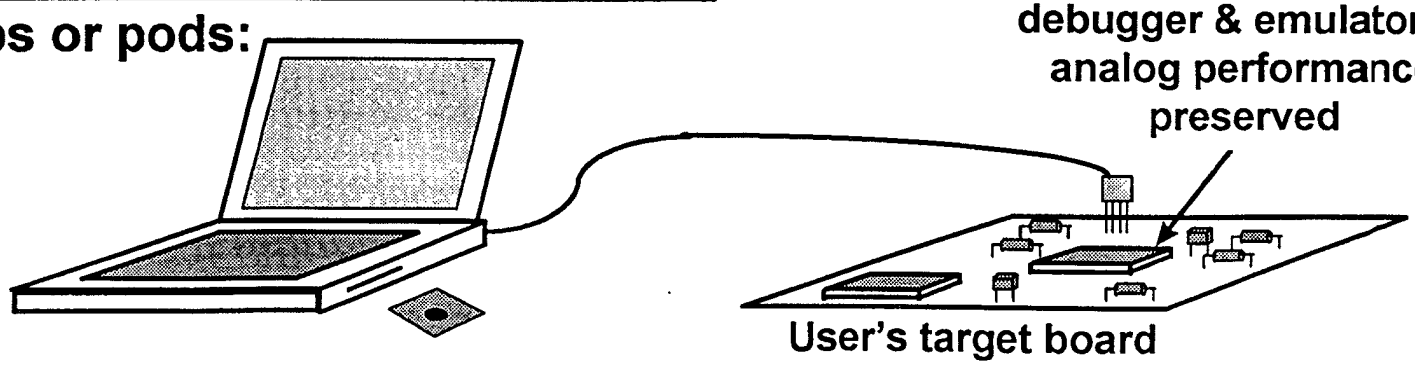
- **Chip has downloader, debugger, emulator on-chip:**

On-chip Downloader:



On-chip in-situ debug/emulation :

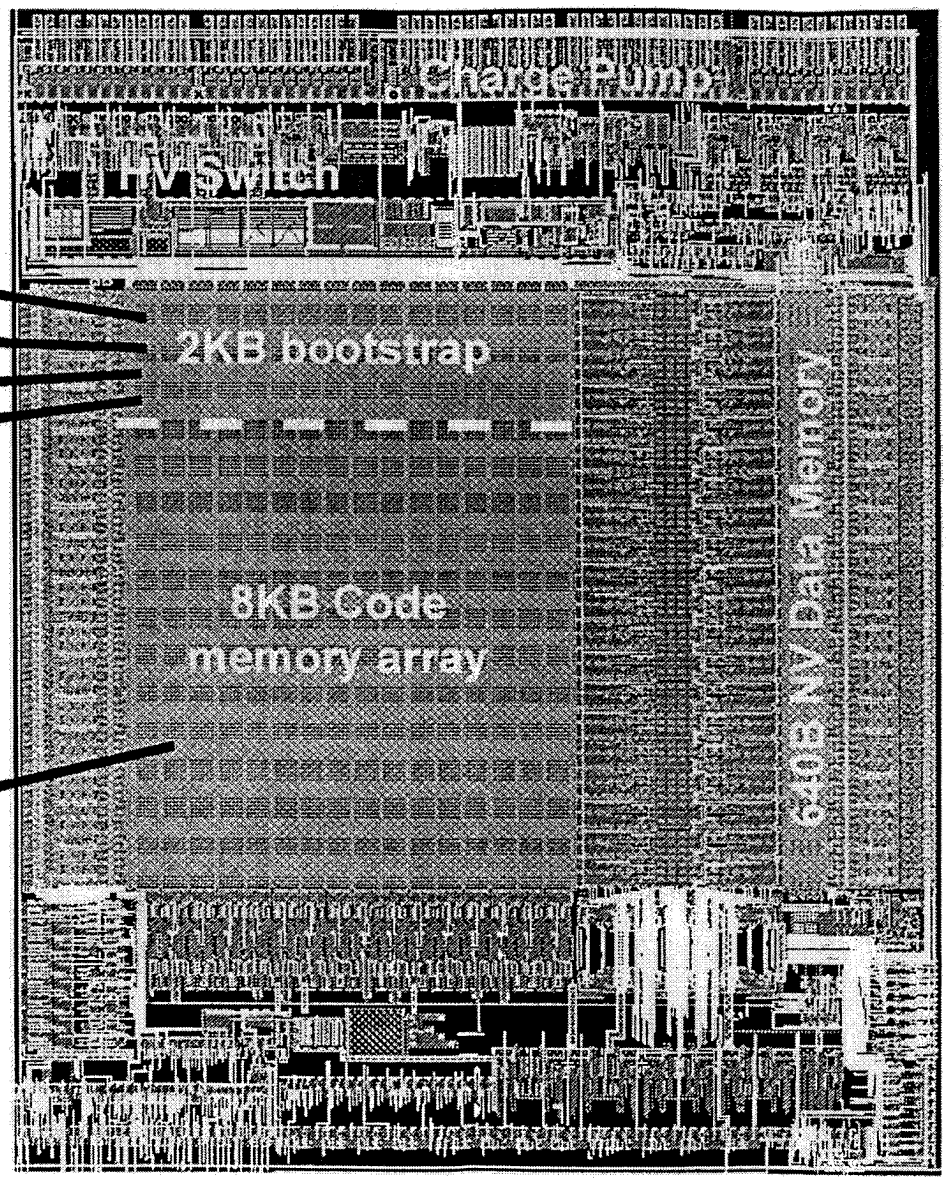
... no clips or pods:



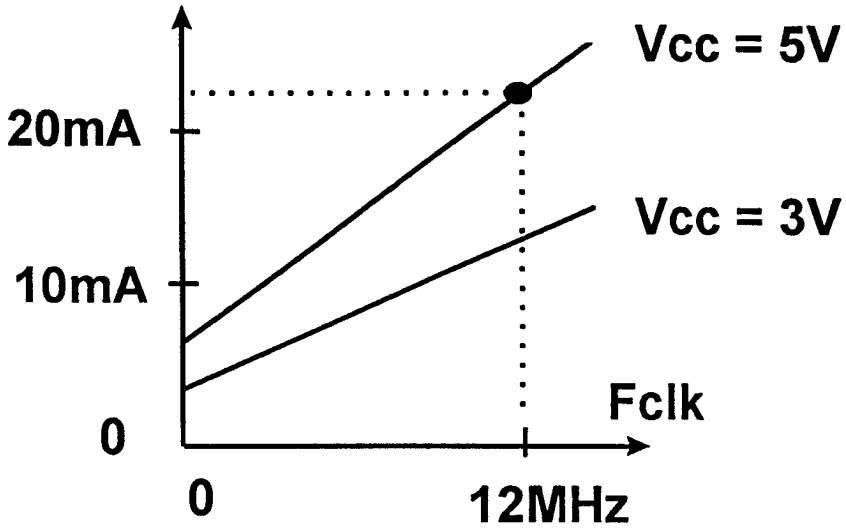
EEPROM Block

Pwr-up loader
Downloader
Debugger
Emulator

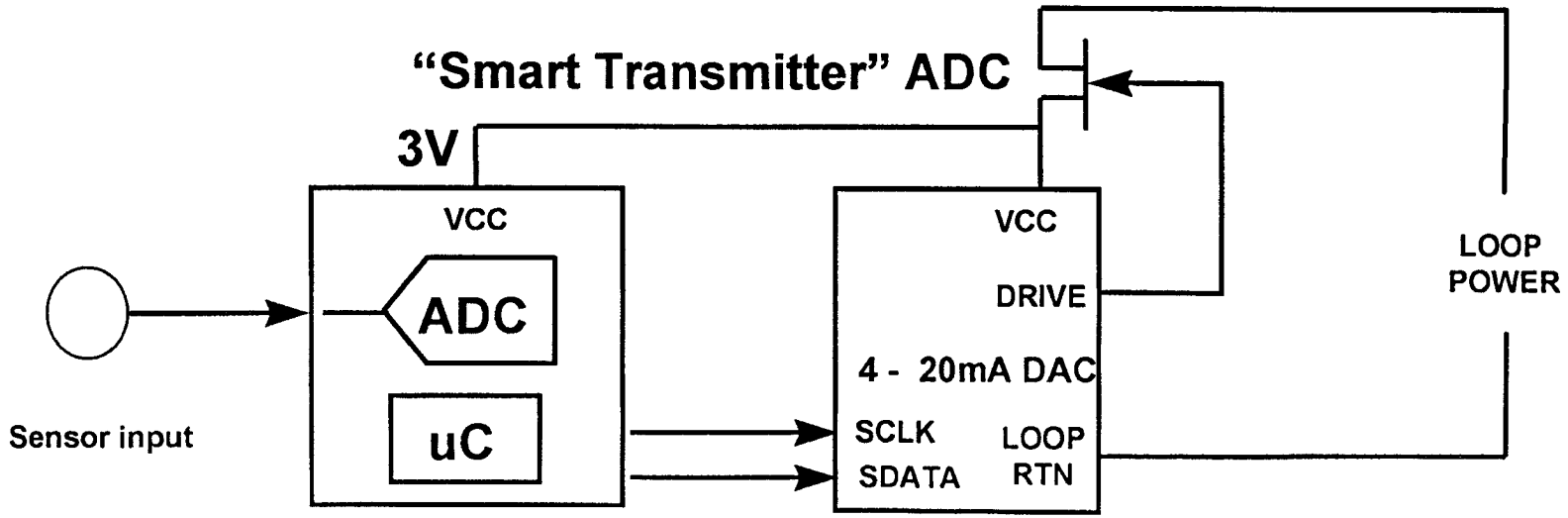
Min Erase sector:
2 rows (64 bytes)



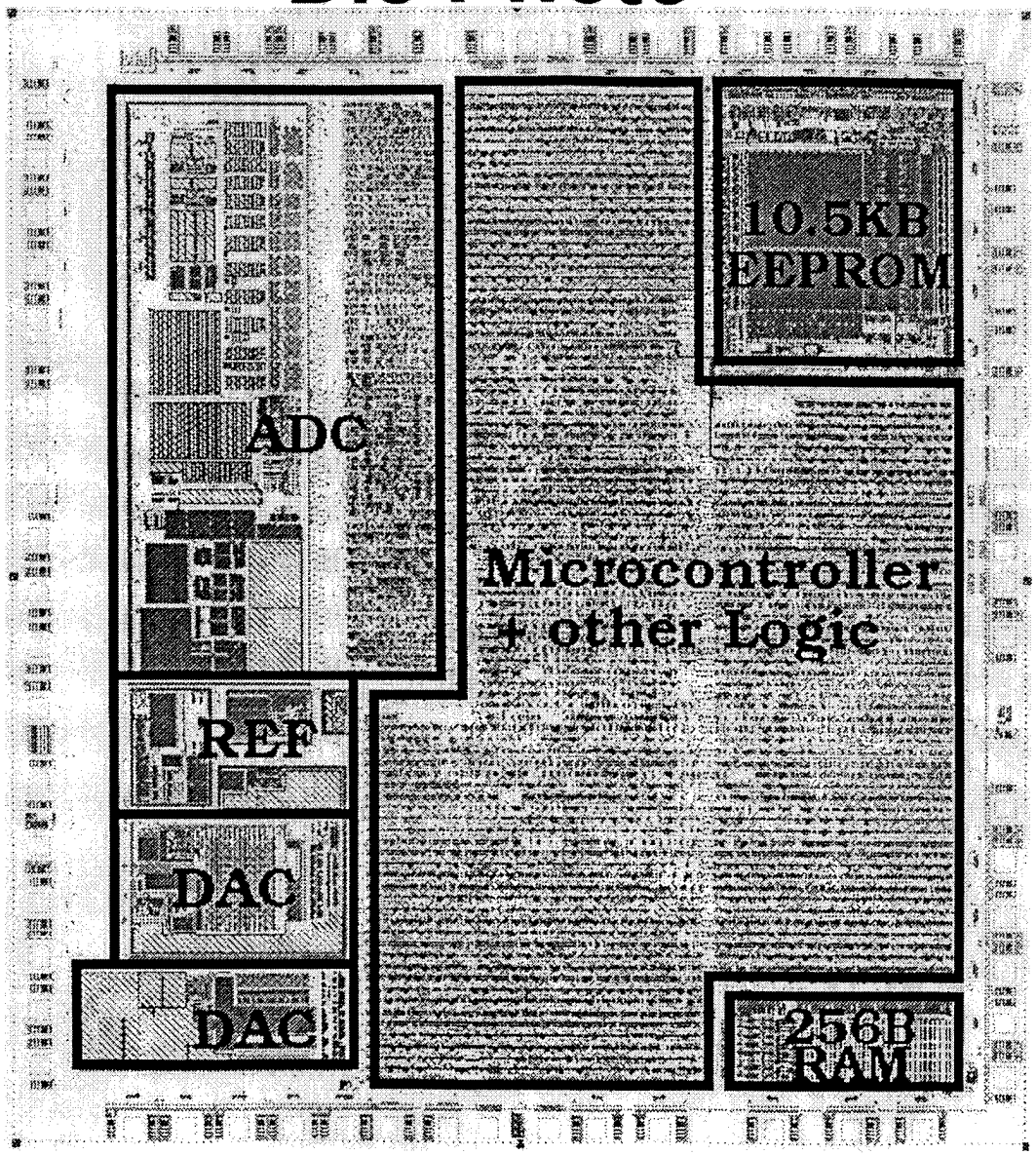
Power Dissipation



25 C,
Dacs Off,
1st silicon



Die Photo



Conclusions

- IEEE 1451 Standard Transducer Interface chip presented - Single chip implementation of 1451 STIM.
- 12b ADC and DACs integrated with uC, Flash EEPROM.
- Metal-Poly caps with calibration and split-gate EEPROM cell simplify process complexity, reducing cost.
- Non-volatile factory or in-situ system calibration - transducer offsets of a few % can be nulled out.
- On-chip down-loader, debugger, emulator ..... no external programmer, emulation H/W, clips,or pods; debug & emulation in-situ preserves analog accuracy.