SA 17.3: An IEEE1451 Standard Transducer Interface Chip

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The IEEE 1451 standard standardizes the interface and communication protocol between networked host control systems and various types of sensors and transducers [1]. The standard transducer interface module (STIM) portion contains the sensor interface electronics, signal conditioning and conversion, calibration, linearization, basic communication capability, and a non-volatile (NV) 565B transducer electronic data sheet (TEDS). Some present microcontrollers with integrated 8 or 10b ADCs or comparator-based slope conversion can implement most of the STIM functionality, but have obvious limitations in conversion speed and accuracy. Few have integrated analog conversion together with high-density EEPROM due to the separate additional process complexity requirements of each.

This chip* integrates the key STIM elements with 12b 5µs conversion in a single device, enabling single-chip STIM implementation for applications requiring higher accuracy and/or faster conversion time such as battery monitoring, pressure and temperature measurement, gas monitoring and leak detection (Figure 1, Table 1). The footprint and power of this single-chip implementation enable remote 4-20mA loop-powered smart-transducer applications and co-mounting of the STIM and sensor. A low-complexity split-gate EEPROM cell and metal-poly capacitors with a calibration algorithm in the ADC are key elements in achieving this level of integration [2,3]. A technique used in the DAC achieves 12b DNL in a small area, allowing integration of two DACs, eliminating the need to use valuable timer/counters for more traditional pulse-width-modulated (PWM) analog outputs.

The ADC is a successive approximation register (SAR) type. Its 12b charge-redistribution DAC consists of an MSB array of eight binary weighted capacitors, and a four-bit LSB array (Figure 2). Each of the eight bits in the main array are calibrated by adjusting the value of its capacitor with a binary weighted capacitor-trim array. The offset and gain capacitors can be calibrated. The ADC self-calibrates by sampling Refin, and AGND on alternate phases and nulls out mismatch errors by successively adjusting each capacitor value. The calibration coefficients are then stored and held in registers. The calibration coefficients default to 12b accurate factory numbers that are pre-loaded by the microcontroller during the execution of a power-up loader in the bootstrap memory. These can then be over-ridden if required, by a software-controlled in-situ calibration, giving the end-user the capability of nulling out not just ADC errors, but also system errors such as offset in a transducer. The input multiplexer can accept eight analog inputs, and has a ninth channel which selects the on-chip temperature sensor. This is a CTAT voltage derived from the on-chip bandgap reference.

Figure 3 shows the 12b DAC multiplying string architecture with buffered voltage o/p. It uses poly resistors, with a main DAC of 64 resistors (6 MSBs) and a sub-DAC (6 LSBs). Previous string DACs use area and power-consuming buffers between the main DAC and sub-DAC to eliminate loading errors that become significant at higher resolutions [4]. This DAC eliminates these buffers using this error. With a main DAC resistance of 40kΩ, and a sub-DAC resistance of approximately 80kΩ, and correctly-sized coupling switches, the loading error comes out as exactly 1 LSB. This step-error is used as part of the DAC transfer function by using 2^{N-1} sub-DAC resistors. In this case 63 resistors are used instead of 64.

The split-gate EEPROM cell is programmed by channel hot-electron injection from the source, and is erased by Fowler-Nordheim tunnelling between the floating-gate poly and control-gate poly (Figure 5). Poly-poly erase eliminates the need for more complex tunnel-oxide processing and drain engineering as required for erase in other EEPROM technologies, making this cell a simple modular addition to a standard CMOS process. The additional steps are a second gate oxide, floating-gate, and three additional implant masks for the 15V and 20V devices in the charge pump and HV switches. Since both program and erase are self-limiting, there is no need for the complicated control logic to prevent over-erase as required in other NV technologies. The 640B NV TEDS data memory is laid out a 320 x 16b array giving a minimum erase sector size of 32b or 4B. This small sector size facilitates software data manipulation, and also increases endurance since each byte sees only one disturb due to programming of a neighboring byte on the same row. The sector in the main 8kB array is 64B.

The bootstrap memory is an additional 2kB EEPROM containing functions such as power-up initialization, serial downloader, on-chip emulator, and various manufacturer ID and calibration coefficients. The serial downloader accepts new program hex code over the UART serial port, starts up the charge pumps, erases the 8k code memory area and then programs the new code. In-situ self-programming and in-situ calibration with nulling of transducer offset and gain errors provide significant new capability for code-upgrades and re-calibration of transducers in remote or inaccessible locations. The ability to self-program is also used by the on-chip emulation to program break-points (jump-to-emulation instruction) into the code-memory area, i.e., software breakpoints with no hardware overhead. This further enables in-situ full-speed emulation with no external clips or pods.

Acknowledgments:

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References:

[1] IEEE Inc., "A Smart Transducer Interface for Sensors and Actuators," IEEE 1451.2 Standard, July 25, 1997.

[2] Yeh, B., "Split Gate Single Transistor Non-Volatile Electrically Alterable Memory Device," US Patent 5,242,848, Sept. 7, 1993.

[3] Cotter, M., P. Garavan, "Analog-to-digital conversion with multiple charge balance conversions", US Patent 5,621,409, Apr. 15, 1997.

[4] Tuthill, M. "High Resolution Digital-to-Analog Converter," US Patent 4,338,591, July 6, 1982.

[5] 3-Soft/Mentor Graphics, "M8052 Macrocell Data Sheet," 1997.

*ADuC812

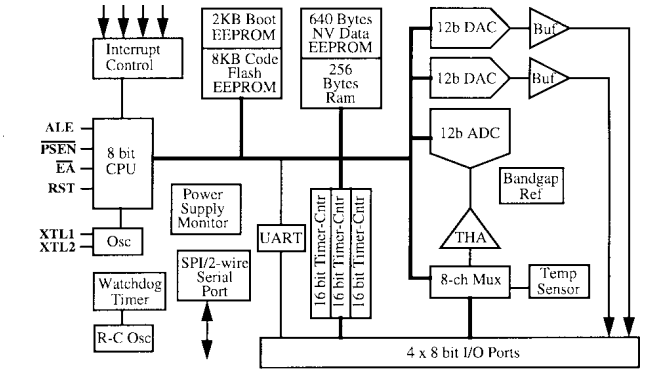

Figure 1: Chip block diagram.

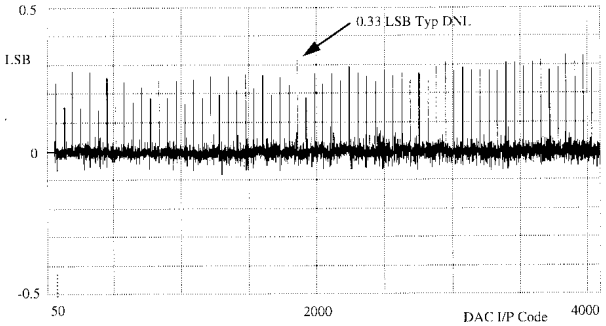

Figure 4: DAC differential non-linearity.

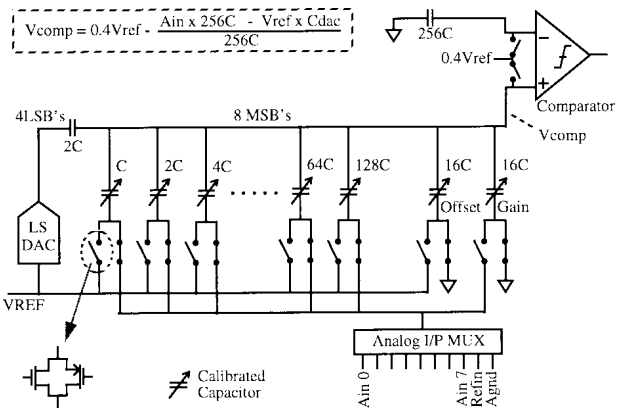

Figure 2: ADC schematic (SAR DAC portion).

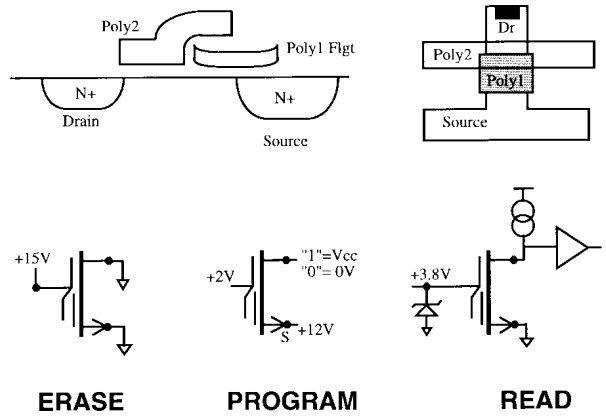

Figure 5: EEPROM cell and operation.

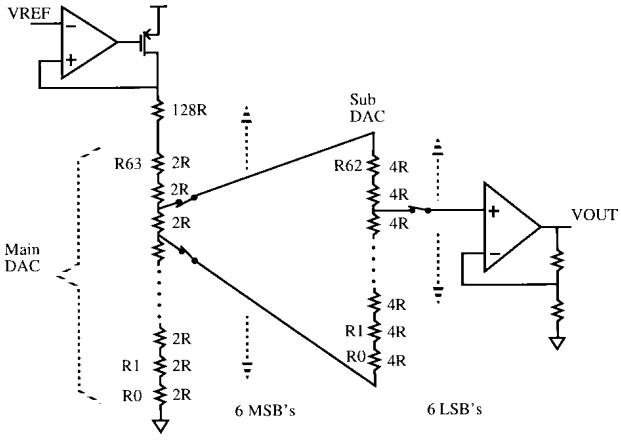

Figure 3: DAC block diagram.

ADC:

8-channel 12-bit 5us SAR
INL: < 1LSB DNL < 1LSB
Temp Sensor = CTAT Voltage
Unit Met-Poly Cap: 14 x 13 um (7.64fF)
Iaa < 1.5mA

DACs:

Resistor String Multiplying 12-bit DAC
Unit poly resistor: 30x1.3 um,154 Ω nom
TConv: 10uS, RL>10KΩ, CL<200pF
DNL: < 1 LSB INL < 4 LSB
Iaa: < 400uA

MISC:

Process: 0.6um CMOS with embedded EEPROM, Two-layer metal.
Die Size: 5.0 x 5.5 mm
Supply: 2.7V - 5.5V single supply
Packages: 44 pin PLCC & 52 pin PQFP

EEPROM:

8KBytes Code Memory
2KBytes Bootstrap/Downloader
640B Non-volatile Data Memory
Cell Size: 4.7 sq.um (0.6u rules)
Program: S=+12V CHE injection
Erase: G=+15V ply-ply FN tunnelling
Endurance: 10K Erase/Prog cycles

MICROCONTROLLER:

Industry Std 8-bit architecture [5]
Four 8-bit I/O ports;
256 Bytes SRAM
7 Interrupts;
Power Supply Monitor
Watchdog timer;
Two Serial Ports
16MHz max Fclk (1.3 MIPS)
Idd = 17mA @ 5V, 12MHz
= 1.6mA @ 3V, 2MHz

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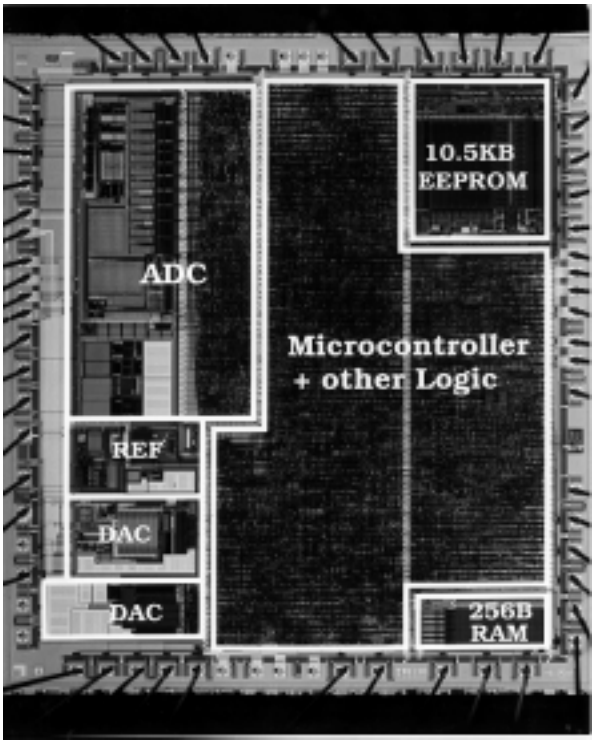

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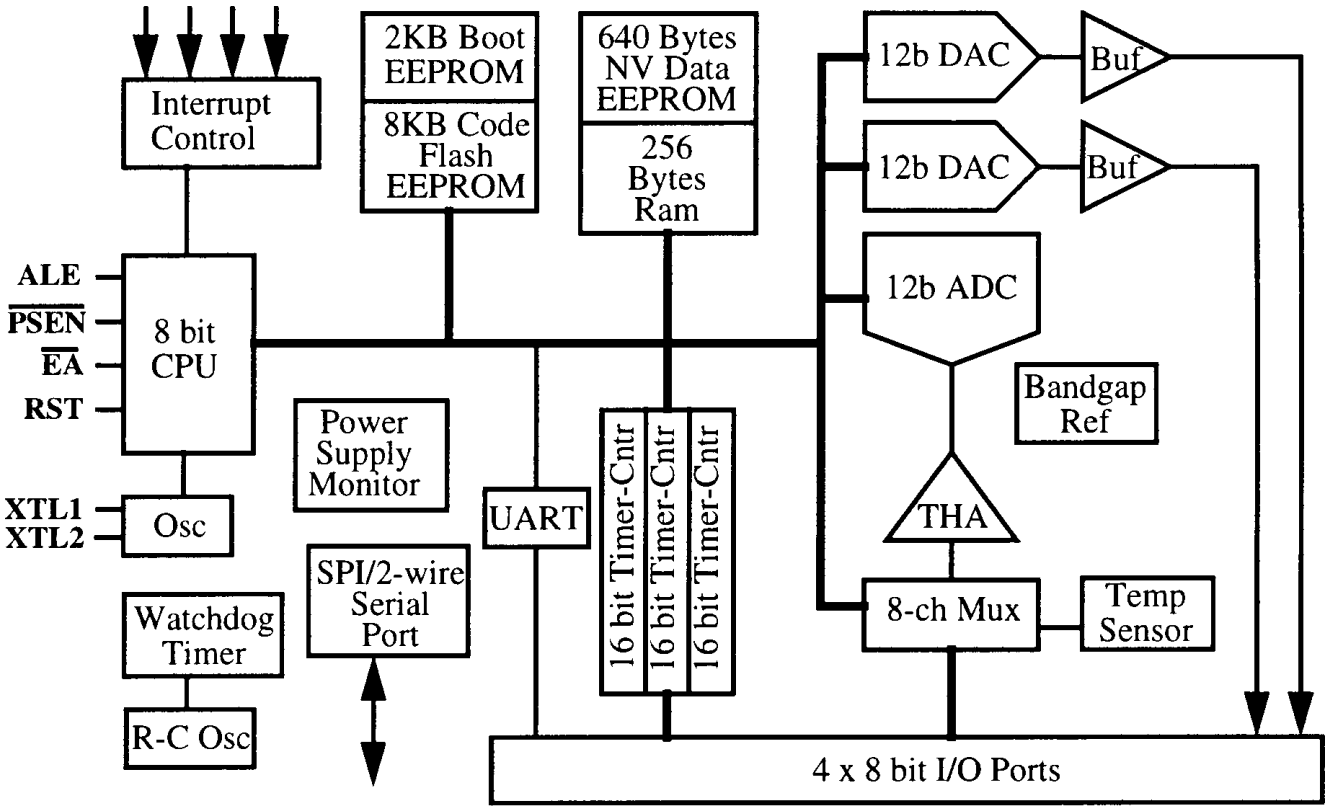
Chip micrograph.



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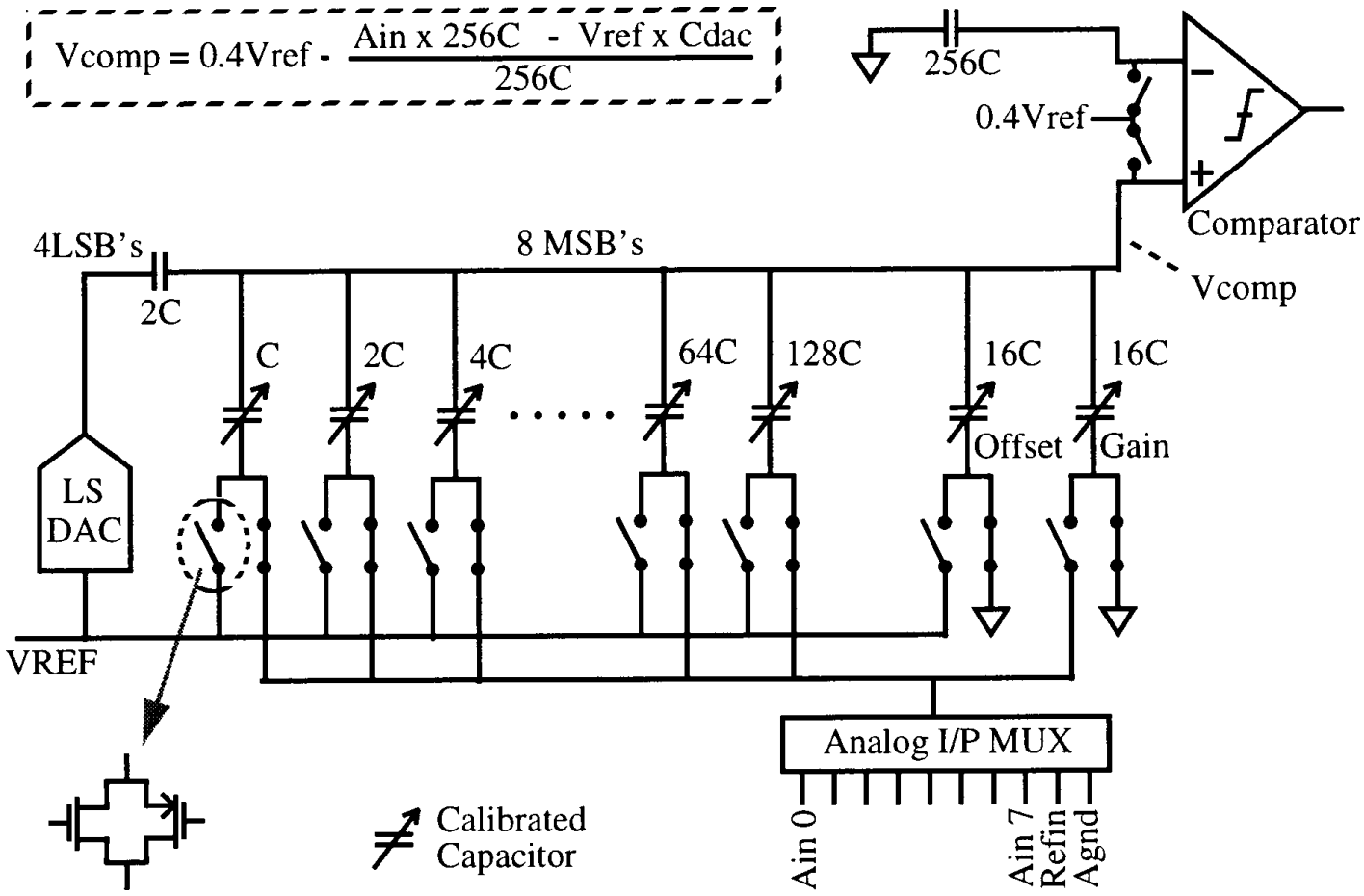

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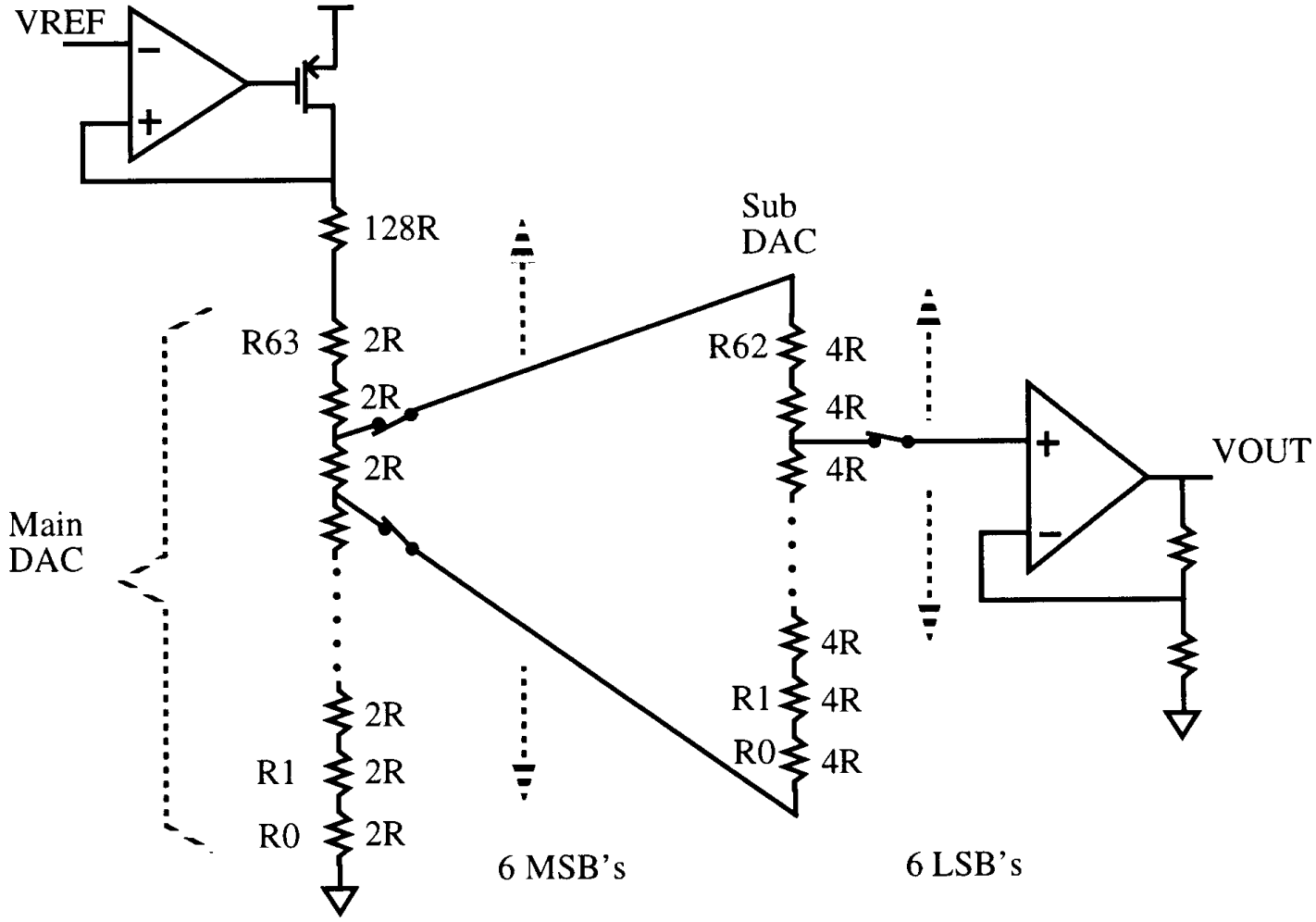

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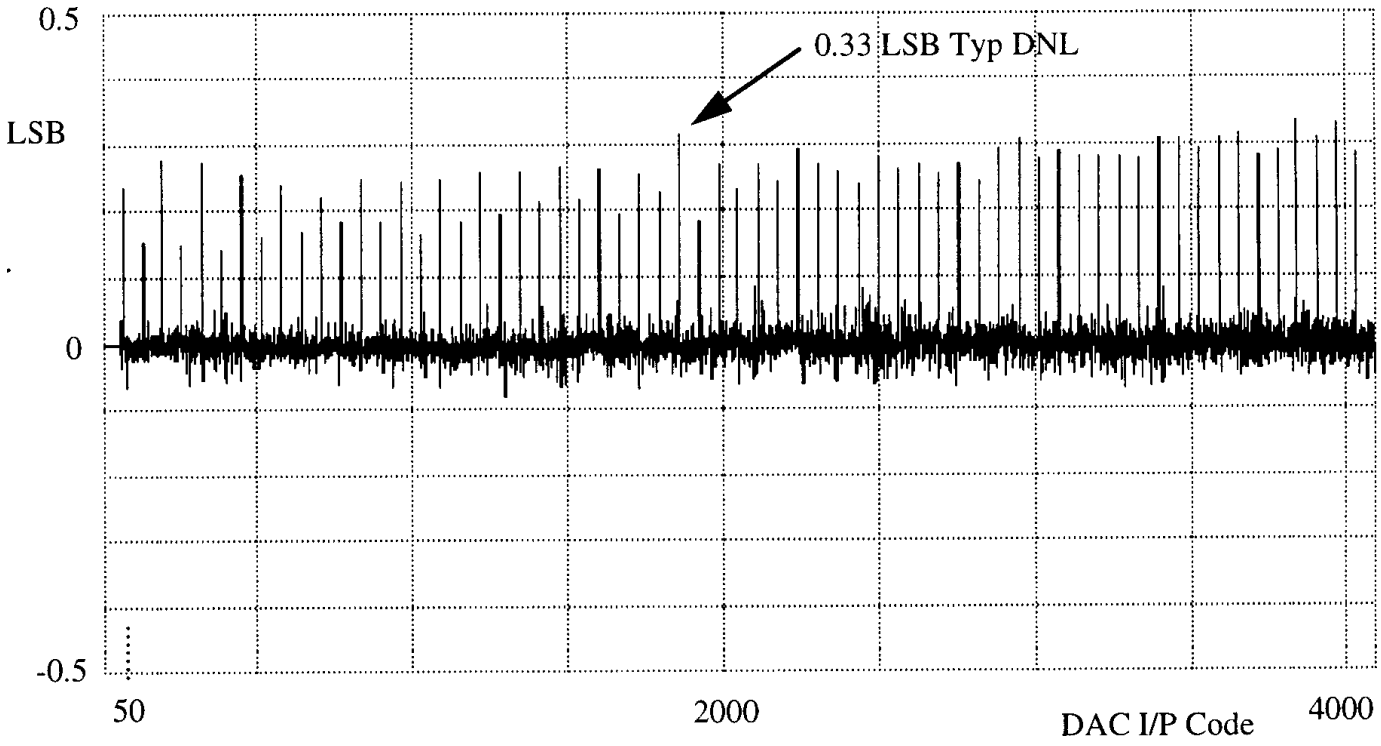

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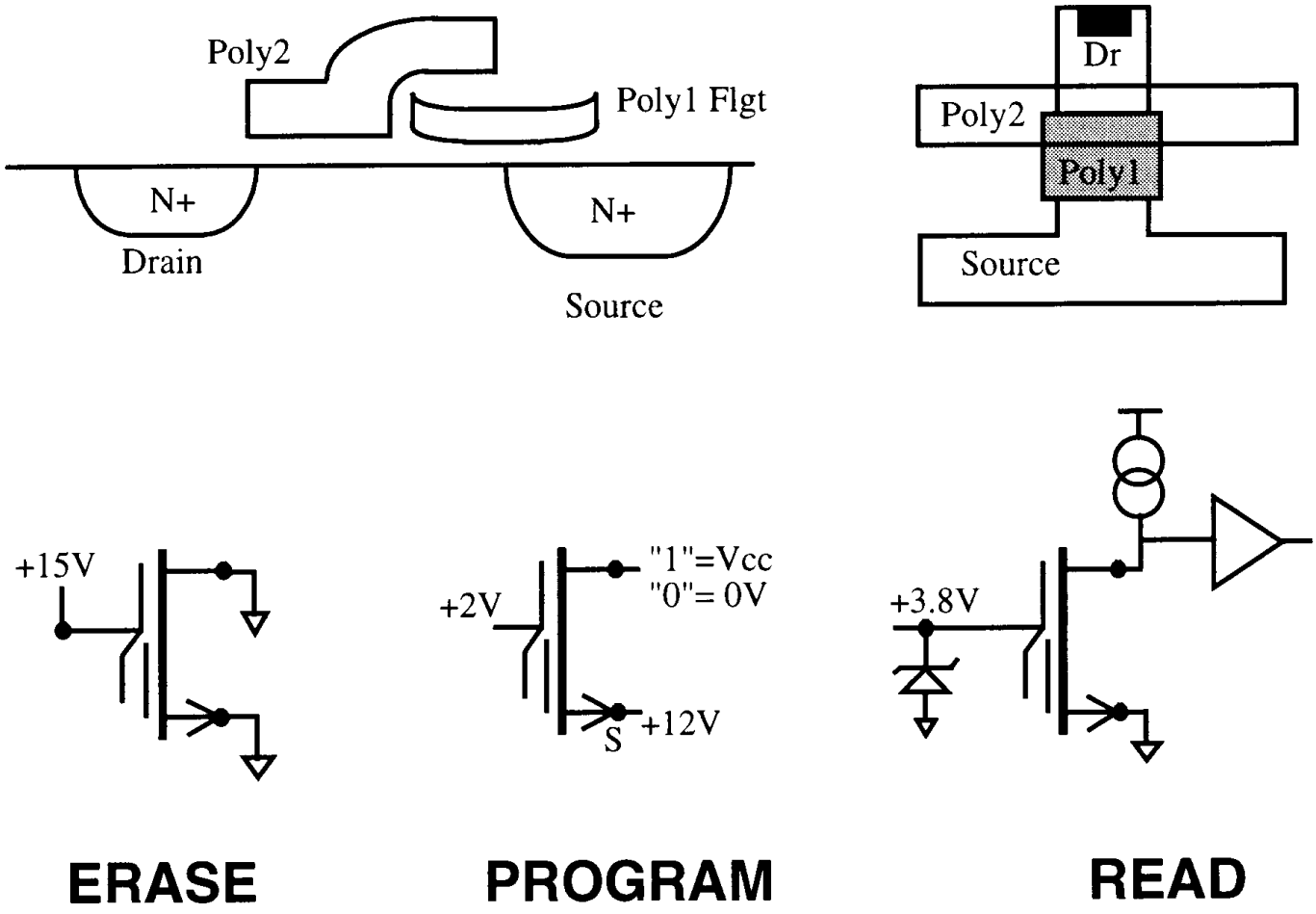

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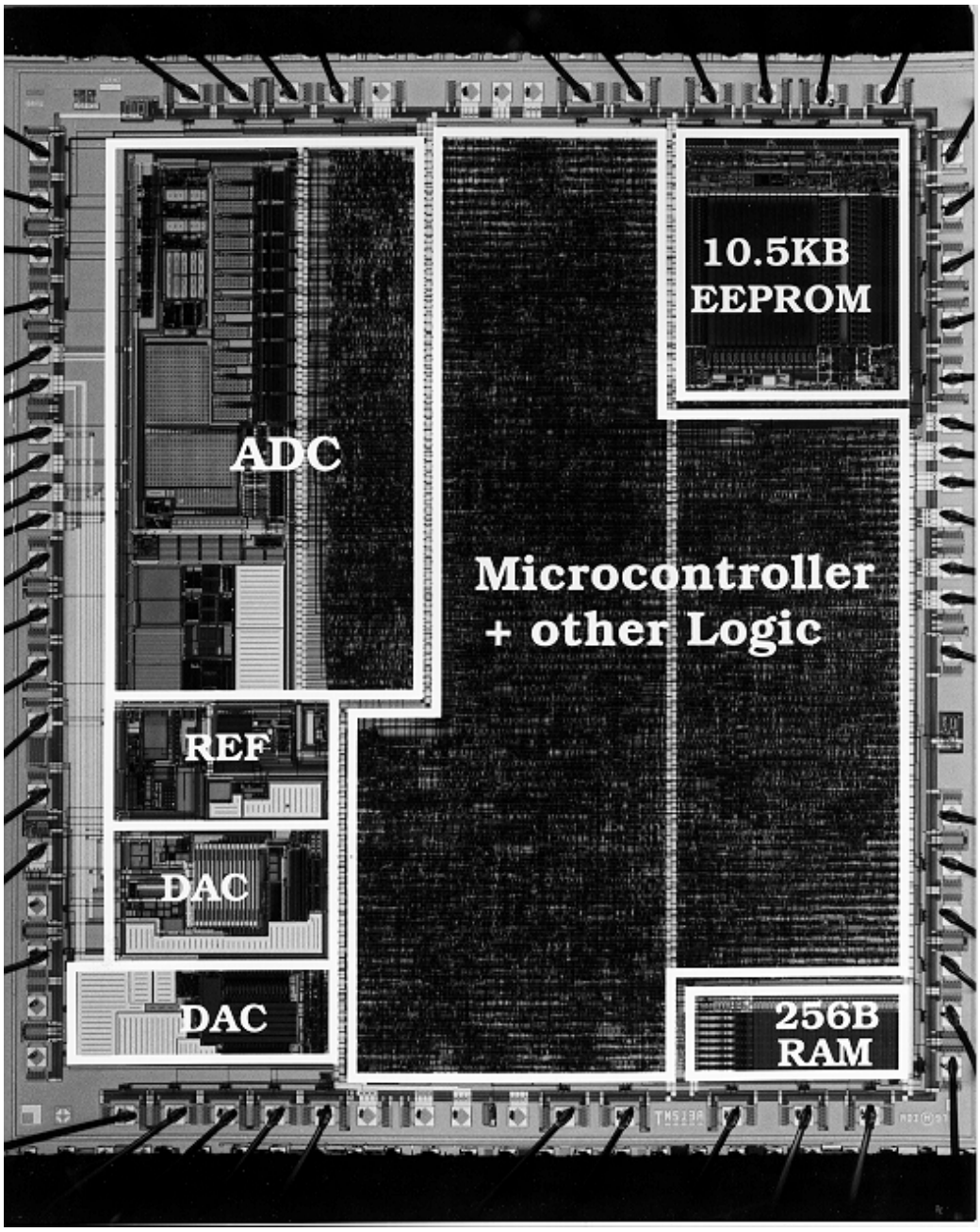

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2KBytes Bootstrap/Downloader
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Erase: G=+15V ply-ply FN tunnelling
Endurance: 10K Erase/Prog cycles

MICROCONTROLLER:

Industry Std 8-bit architecture [5]
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7 Interrupts;
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