2020 15-418/618 Exam 2 Clarifications

Problem 1

- A. Assume the program is executed on an out-of-order processor using one of the memory models listed below.
- F. Compare the nonleaky version to a queue designed for single-threaded execution using the same data structure
- K. Answer the question based on the general properties of ASICs and FPGAs
- O. Use the network designs presented in Lecture 15.

Problem 2

- See the code in the revised handout, showing how the lock is initialized
- (3) should be `lock->serving`, not `next->serving`
- (6) See the Wikipedia entry on the MSI protocol, linked from the exam resources web page.
- (6), (7)(a), (7)(b). Answer these questions as if each of these steps occurred in sequence, and that all involve 8 threads running on 8 cores. You can assume a bus-based implementation.

Problem 3

- A. You should determine the way in which Test 3 fails.
- B, C. Conflict detection is performed at the node level

Problem 4

- All speedups are relative to an unspecified baseline processor. The design of this processor and its resource requirement are not important.
- 4A: Parameter r can be less than 1.0, as long as it is positive.
- 4A(1): Give the speedup in the sequential region only.
- 4A(3): End-to-end mean the entire program execution.
- 4B(5): Use f = 0.9 and N = 16.

Problem 5

- See the code for Figure 5 in the revised handout, correcting the ordering of indices for the global variable `weights`
- P. 18 The formula on the last line should be (K-1) x D_i.
- For problems asking for numbers, you should show how you get these values in the event you may be eligible for partial credit
- B. Assume the machine operates in a SIMD-like fashion, with the threads performing their loads in lock step.