# **Read-Modify-Write Performance in NUMA Architectures** Naama Ben-David and Ziv Scully

#### Benchmark

do	{	
	wait(cr)	
	val = Read(x)	
	<pre>new_val = (myID,</pre>	iter++)
	wait(rc)	
}	<pre>while(!CAS(x, val,</pre>	new_val))

rc (read-to-CAS) delay represents "real work" cr (CAS-to-read) delay is backoff

## NUMA Architecture



#### Intel Xeon Phi 4 nodes 18 cores per node 2 threads per core

AMD Bulldozer

- 8 nodes (2 per socket)
- 4 cores per node
- 2 threads per core

## **Machine Comparison**



#### Node Heterogeneity







Workers using "smart" backoff skip CAS attempt if another worker from their node had the most recent success

#### **Execution Traces**



