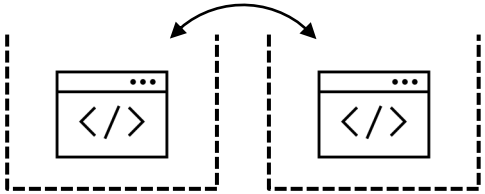
Lord of the Ring(s): Side Channel Attacks on the CPU On-Chip Ring Interconnect Are Practical

Riccardo Paccagnella, Licheng Luo, Christopher W. Fletcher

ILLINOIS

Side Channel Attacks

Side Channel Attacks



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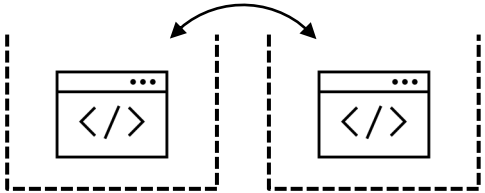

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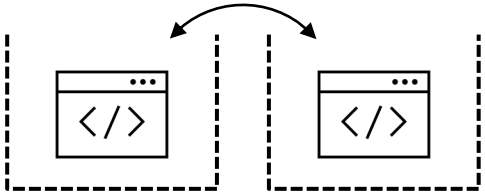

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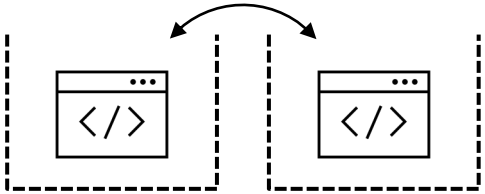

{* SECURITY *}

Google emits data-leaking proof-of-concept Spectre exploit for Intel CPUs to really get everyone's attention

I don't believe it, I had to see it, I came back, I came back haunted

Thomas Claburn in San Francisco Fri 12 Mar 2021 // 21:28 UTC SHARE

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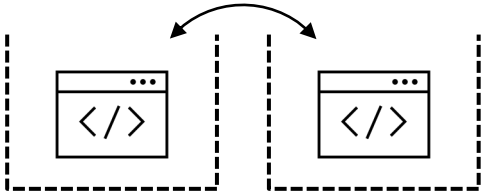

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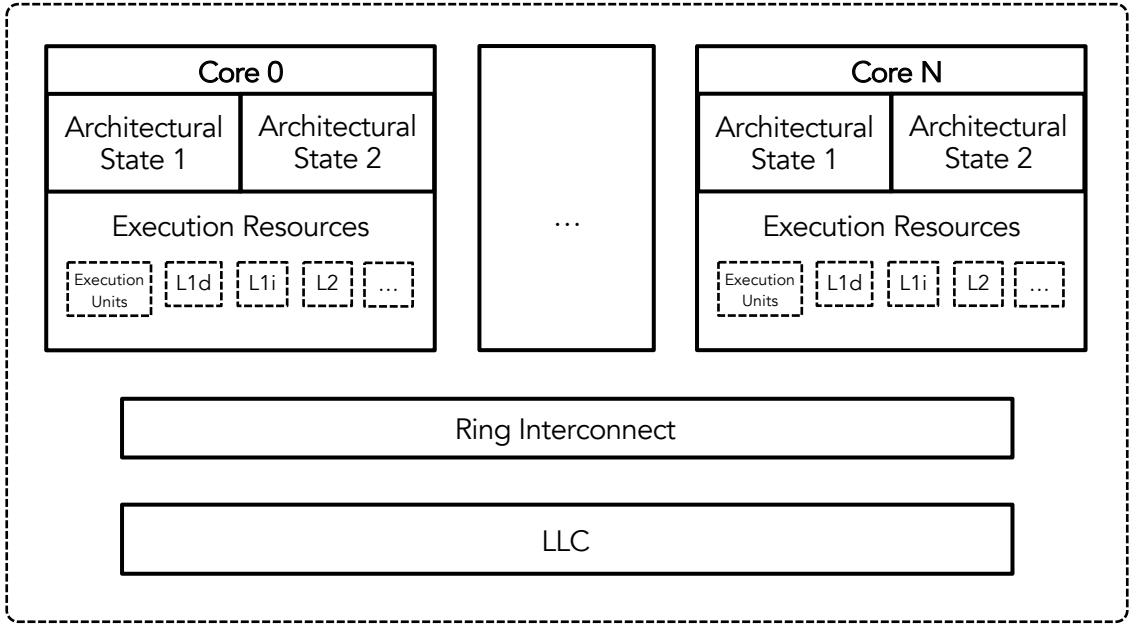

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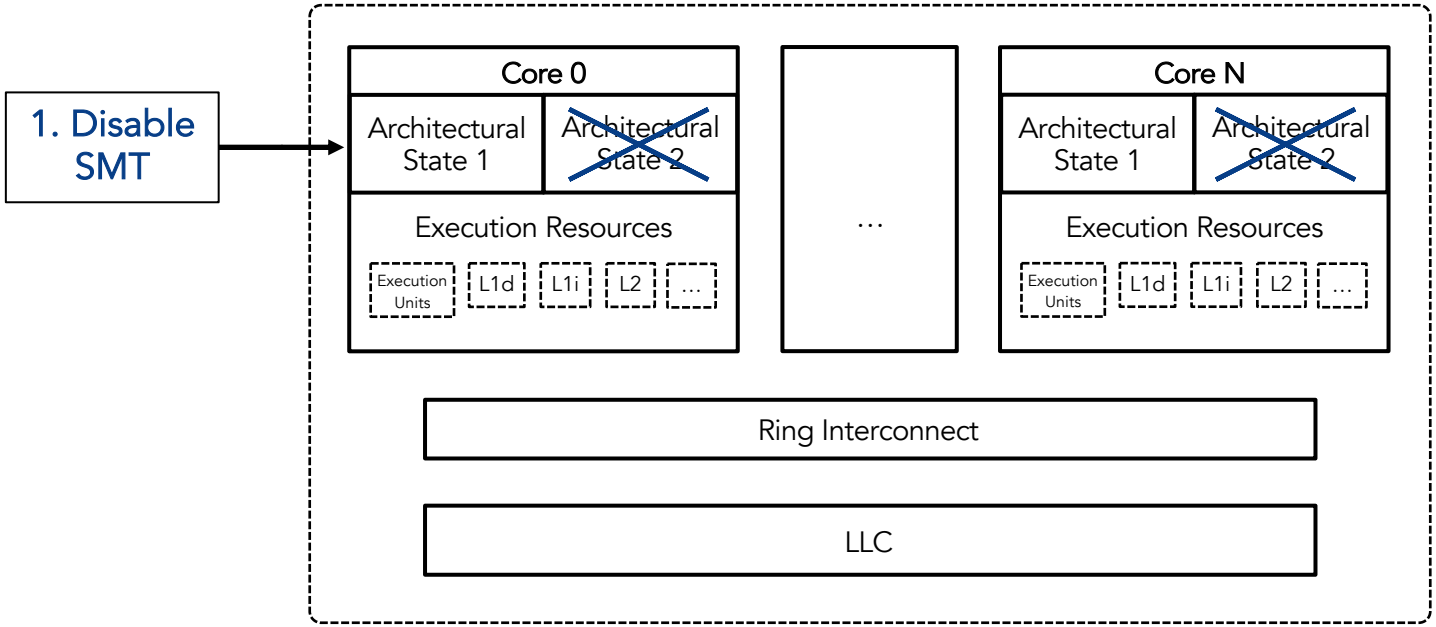

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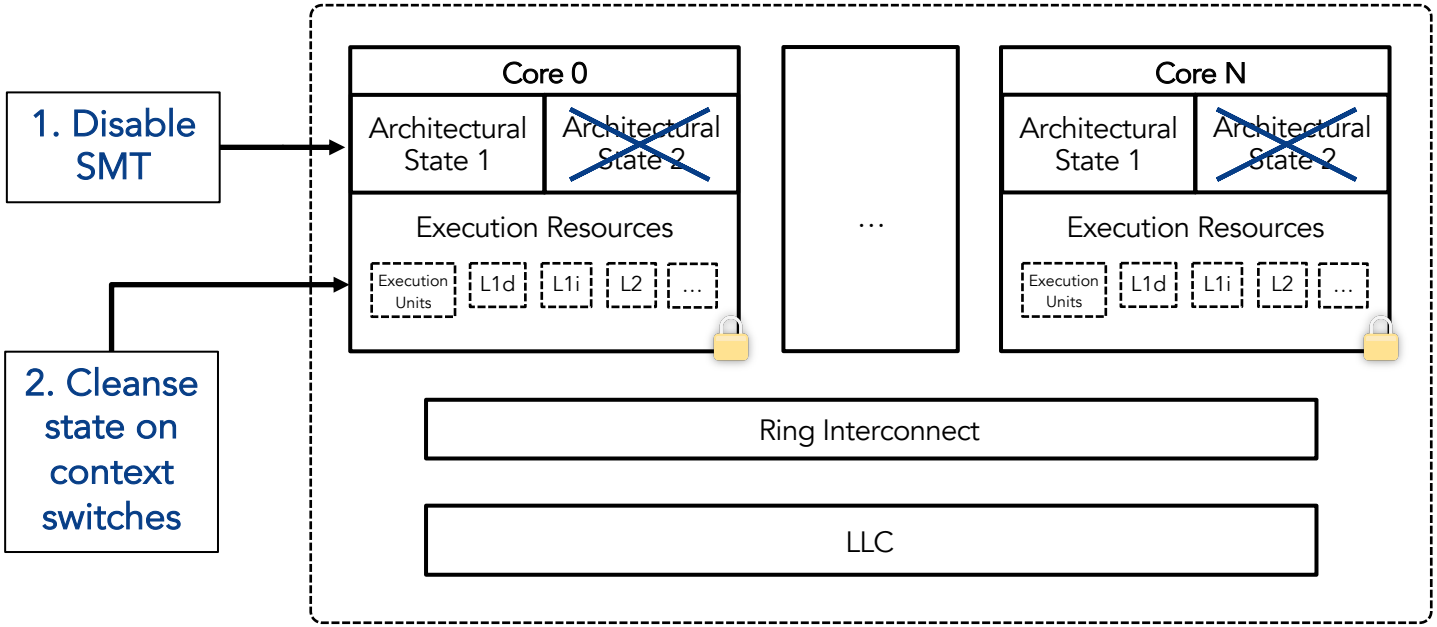

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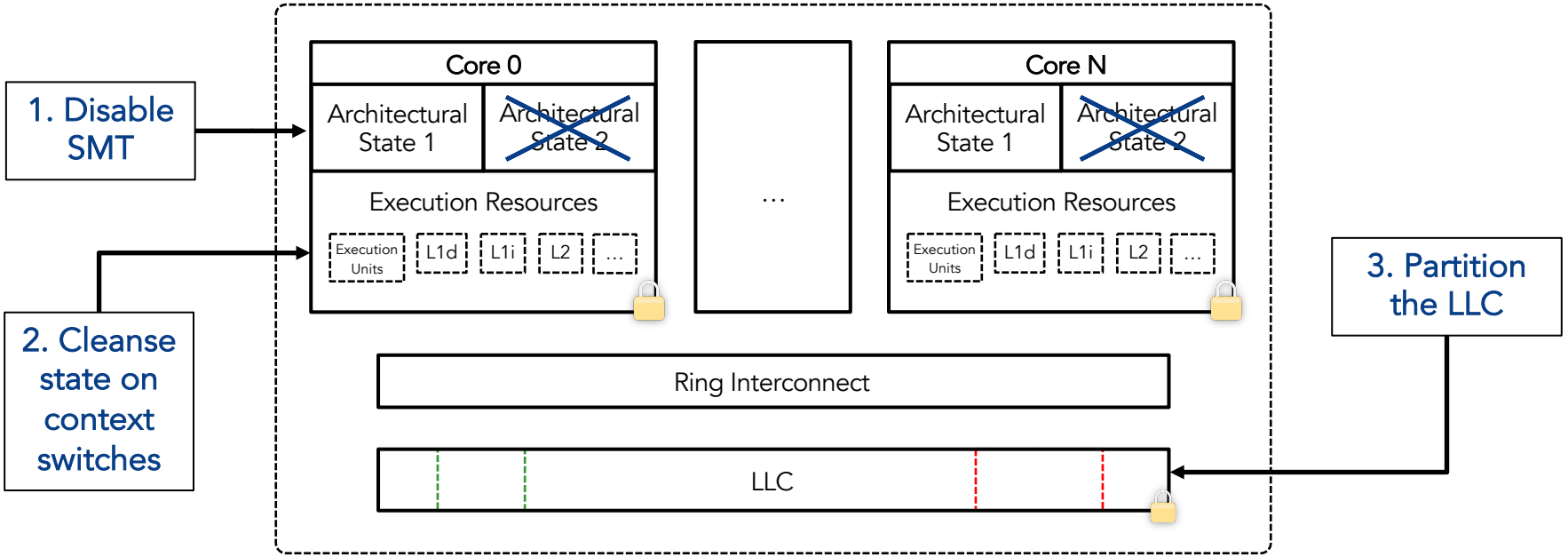
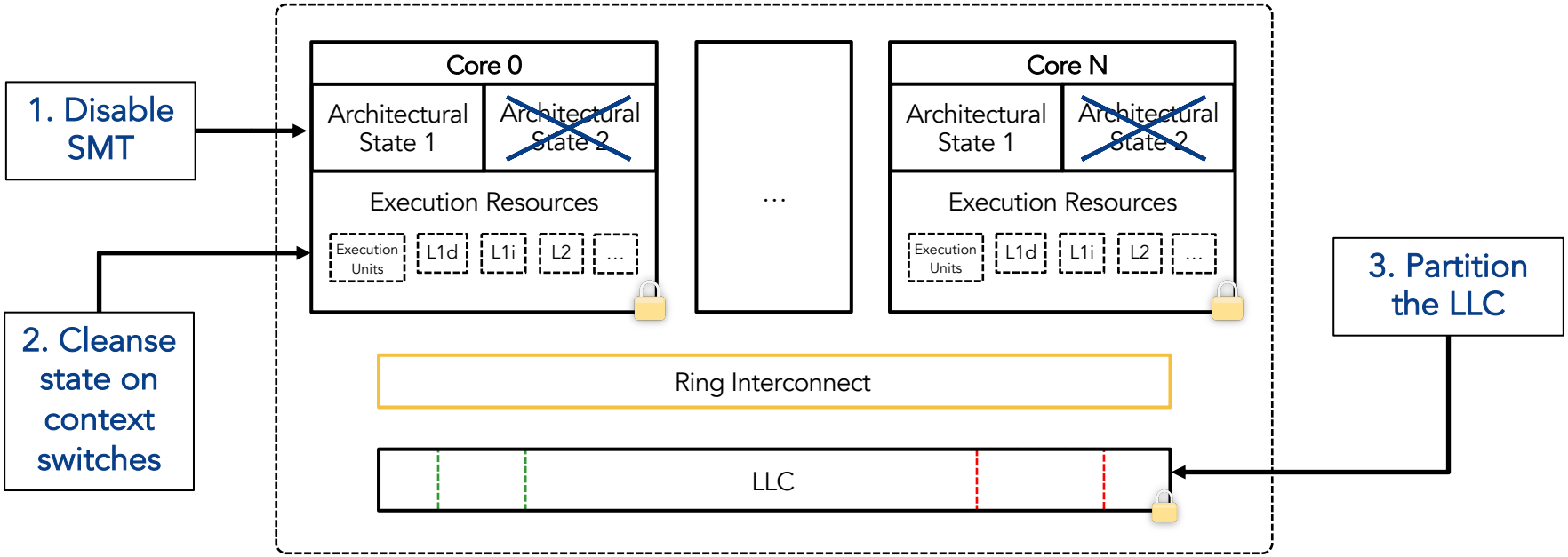
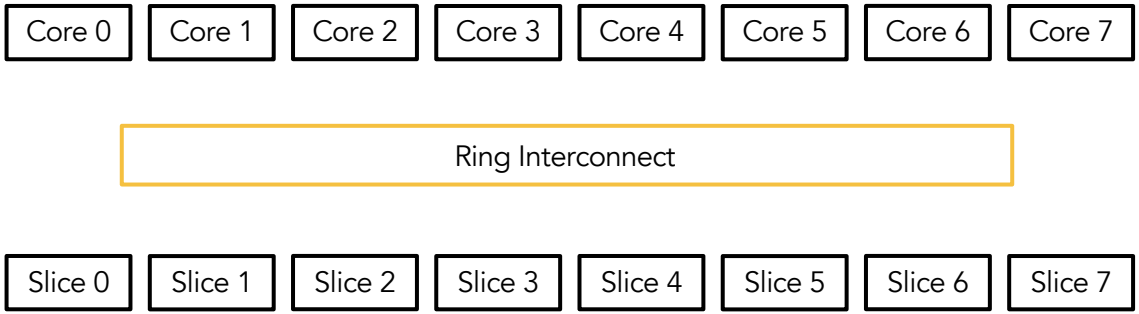


What about the ring interconnect?

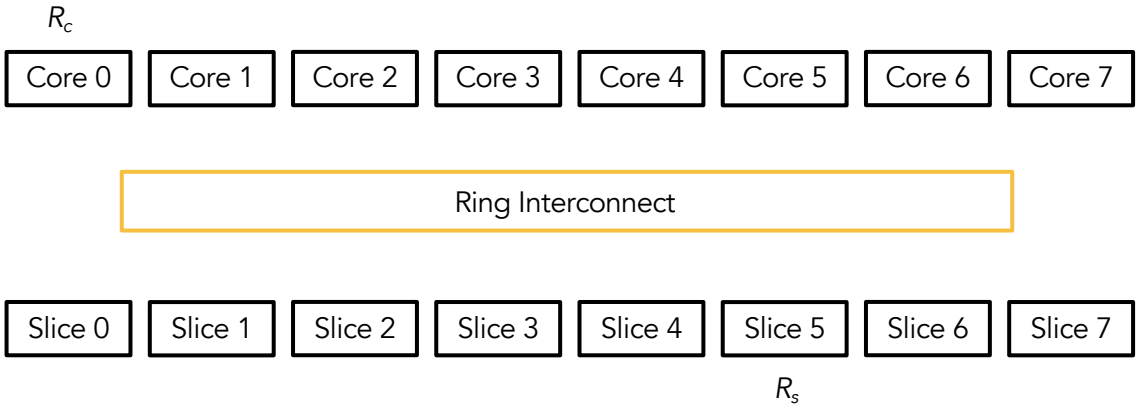


Methodology



Methodology

- R_c = receiver core
- R_s = receiver LLC slice



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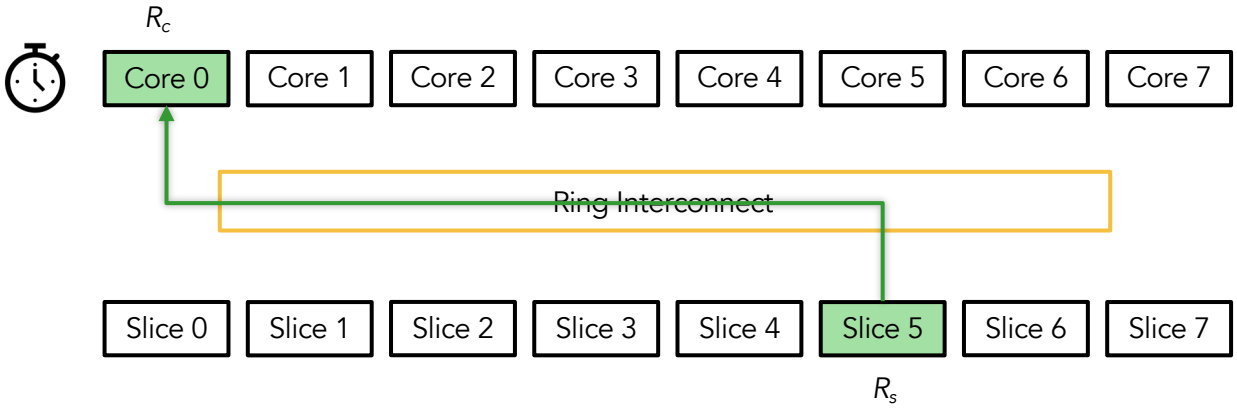

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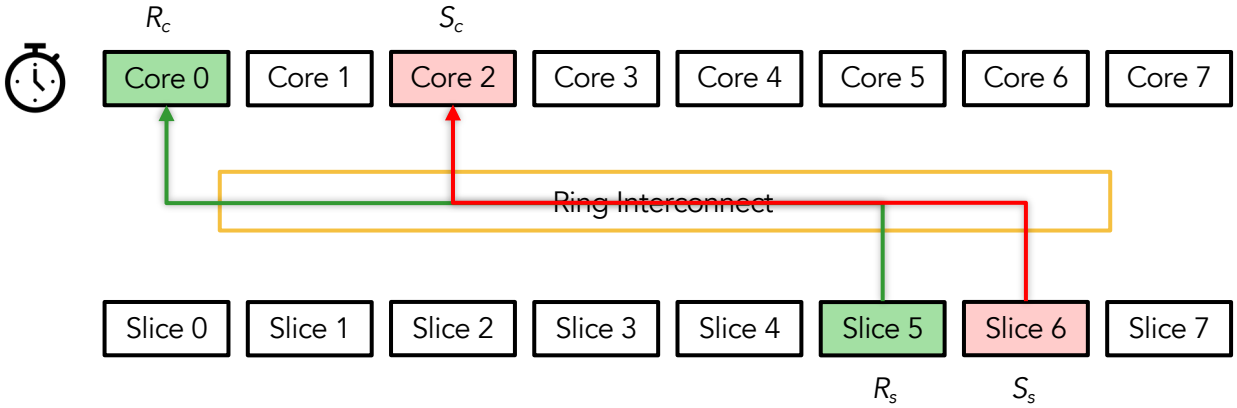
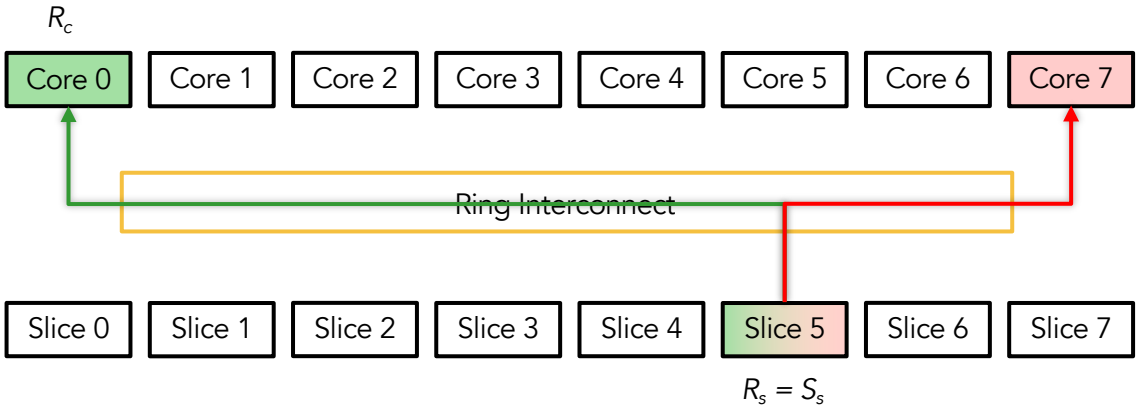


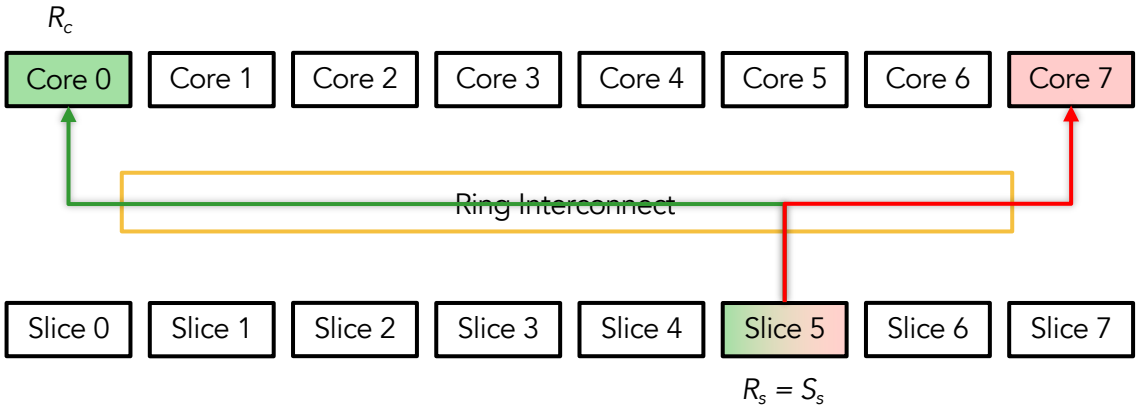
Slice Contention

- $S_s = R_s$: contention



Slice Contention

- $S_s = R_s$: contention
  - Slice's request queue.
  - Slice port.



Ring Stops

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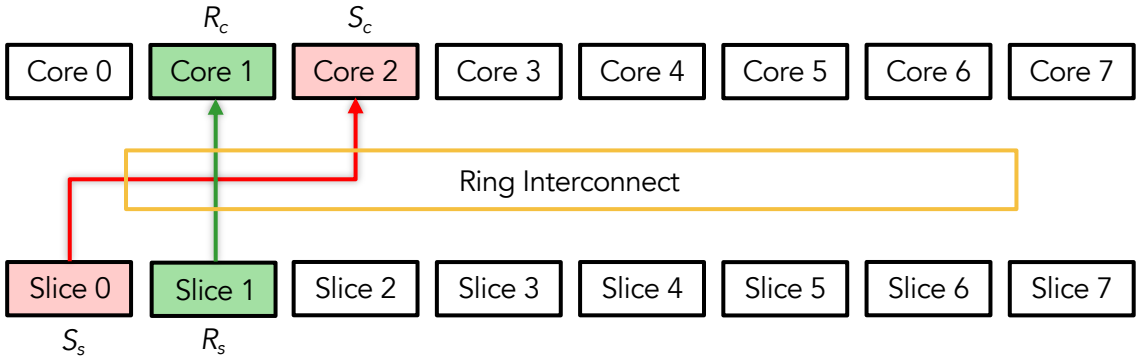
  - Traffic between core *i* and slice *i* does not contend with cross-ring traffic.



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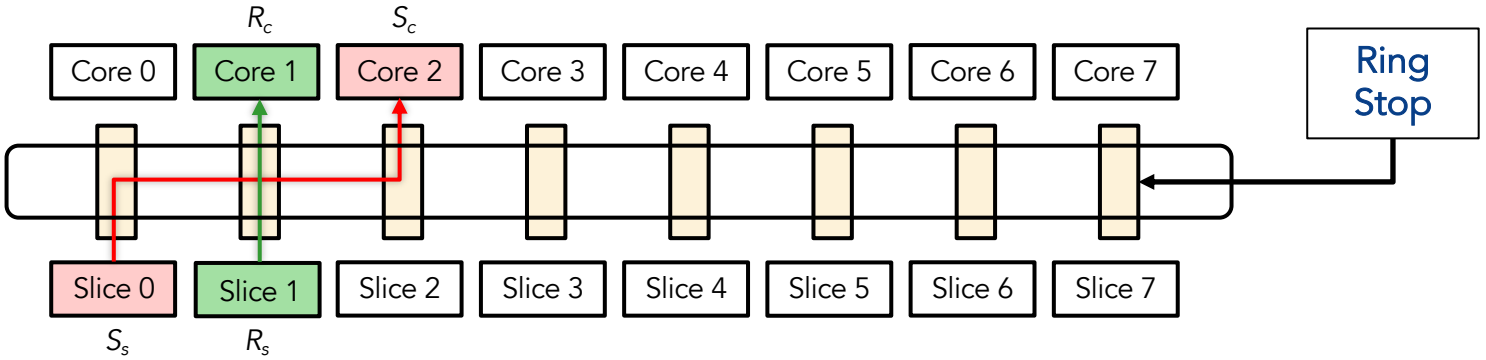

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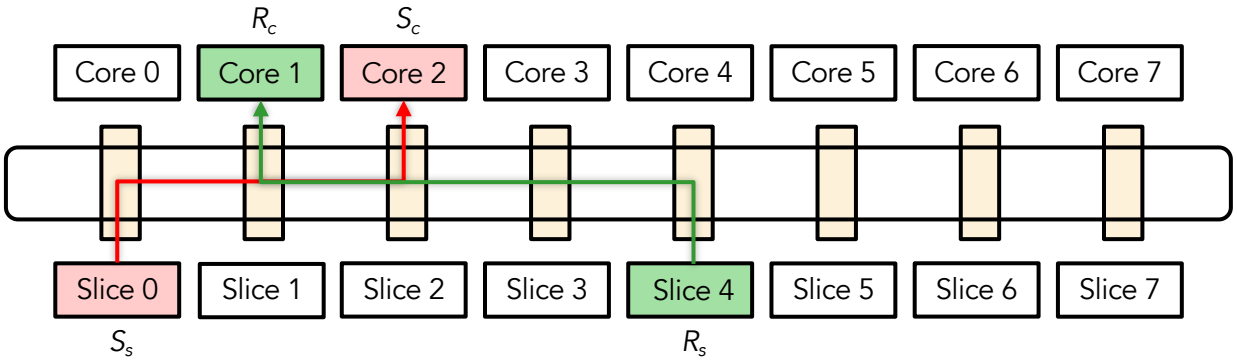

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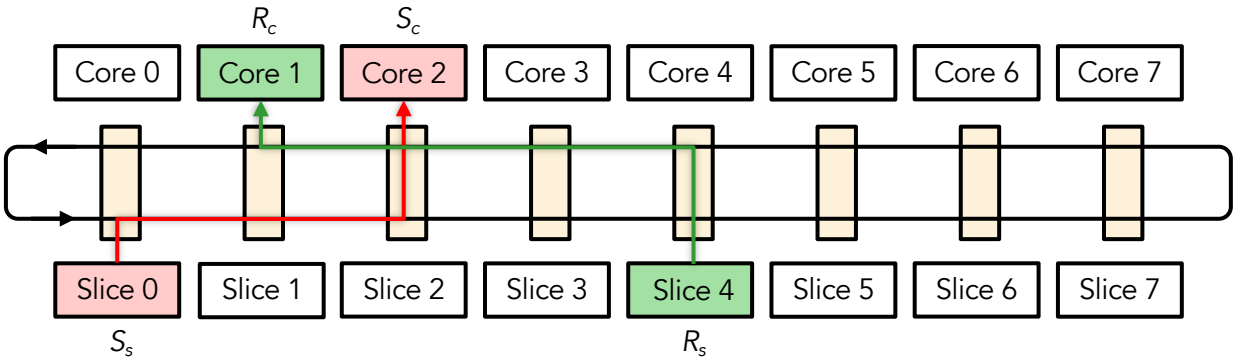

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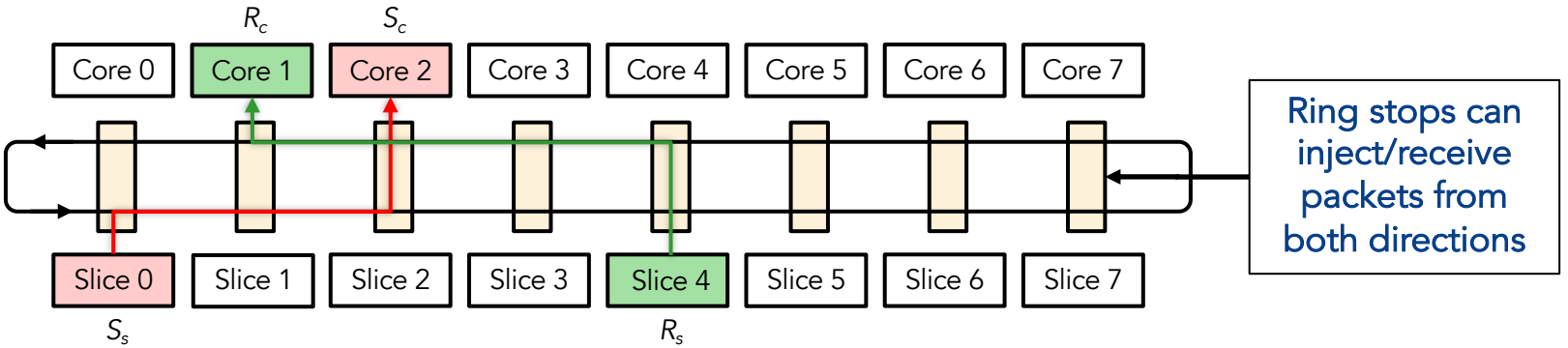
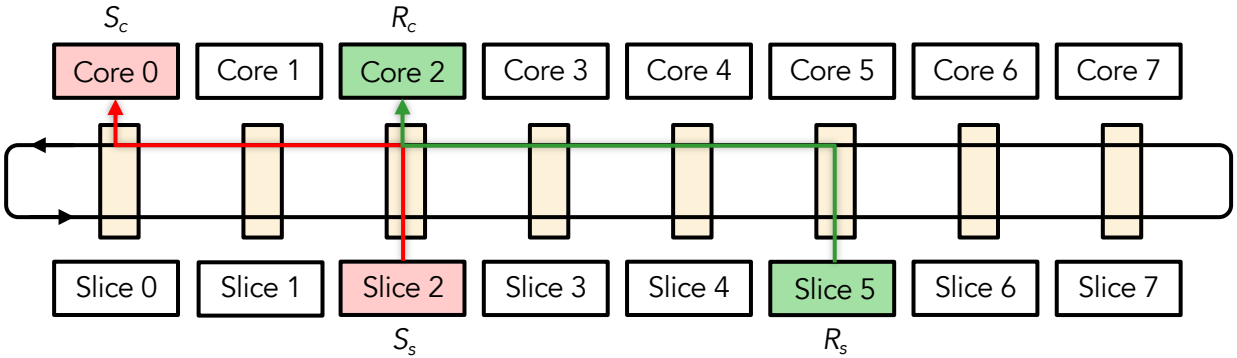


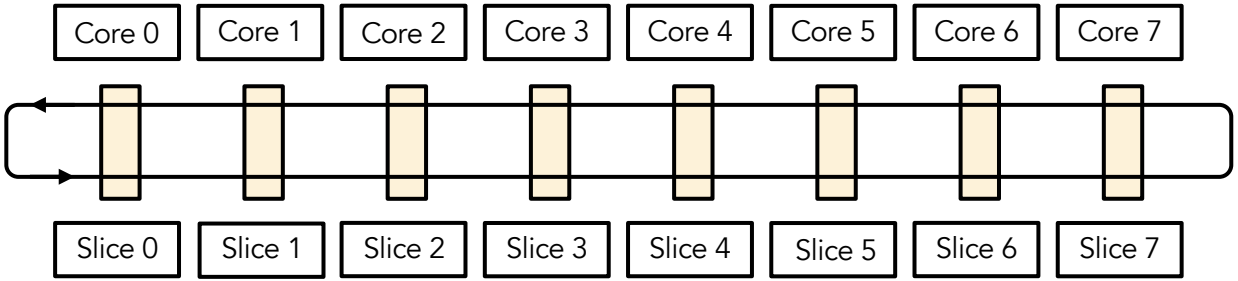
Overlapping Segments

- No overlapping = no contention.
  - Traffic on the ring only travels through the shortest path.



Checkpoint

- So far: ring contention requires overlapping segments + same direction. Surprisingly, these conditions are not sufficient.



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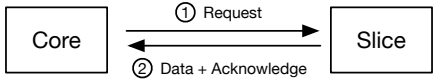
- A clean LLC load uses the request ring, the acknowledge ring and the data ring.



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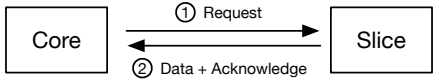

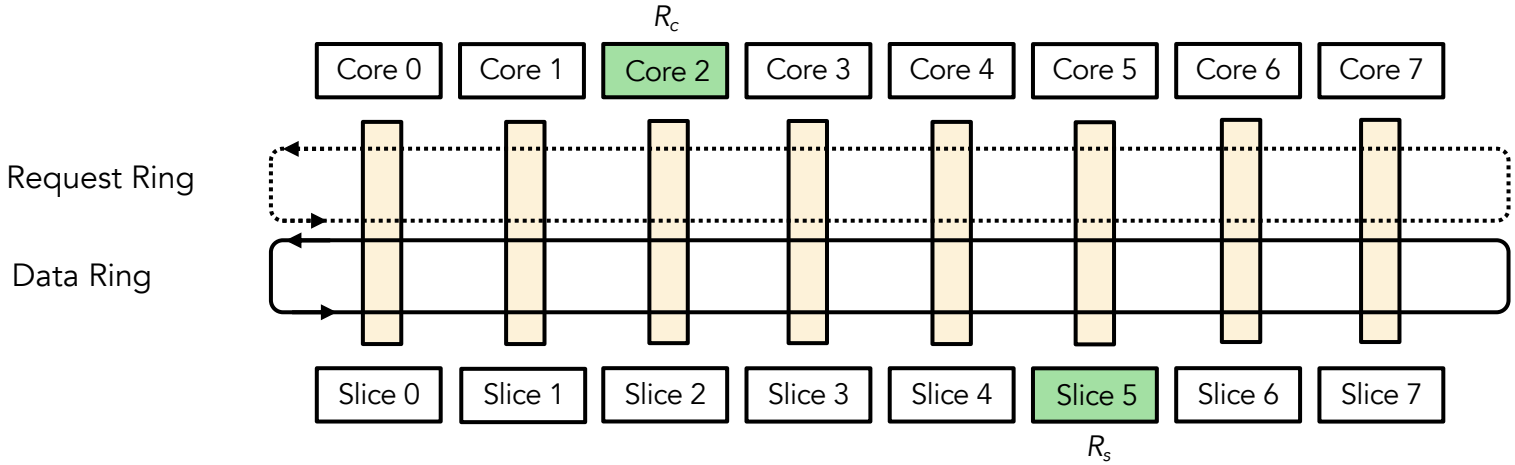

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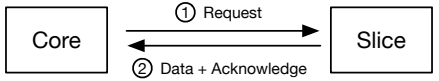

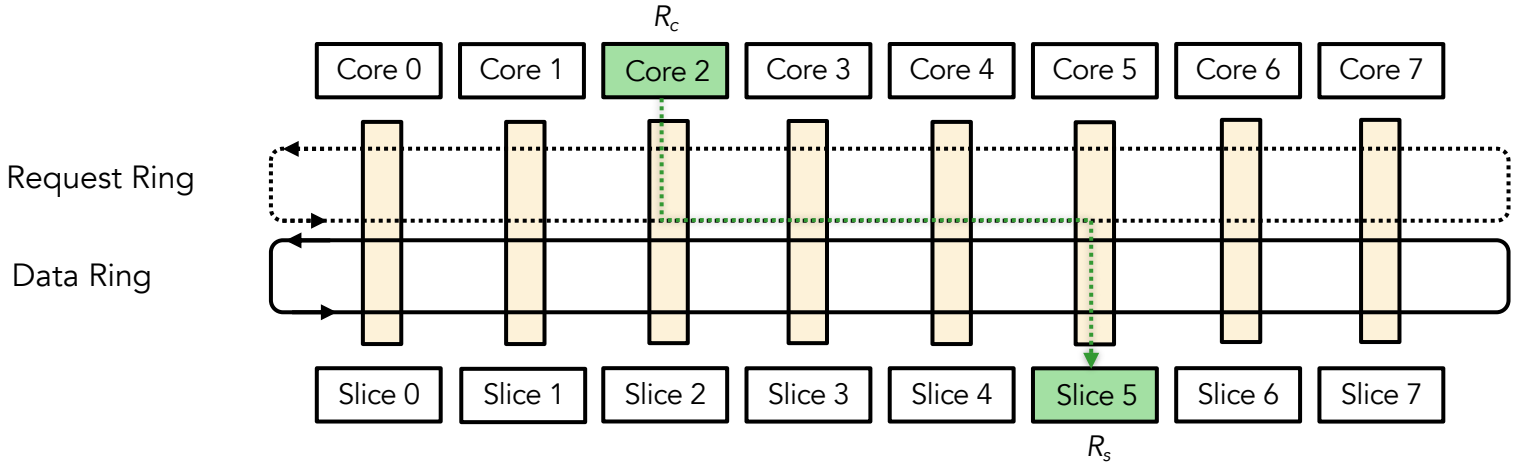

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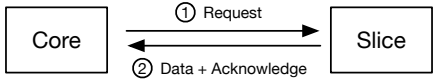
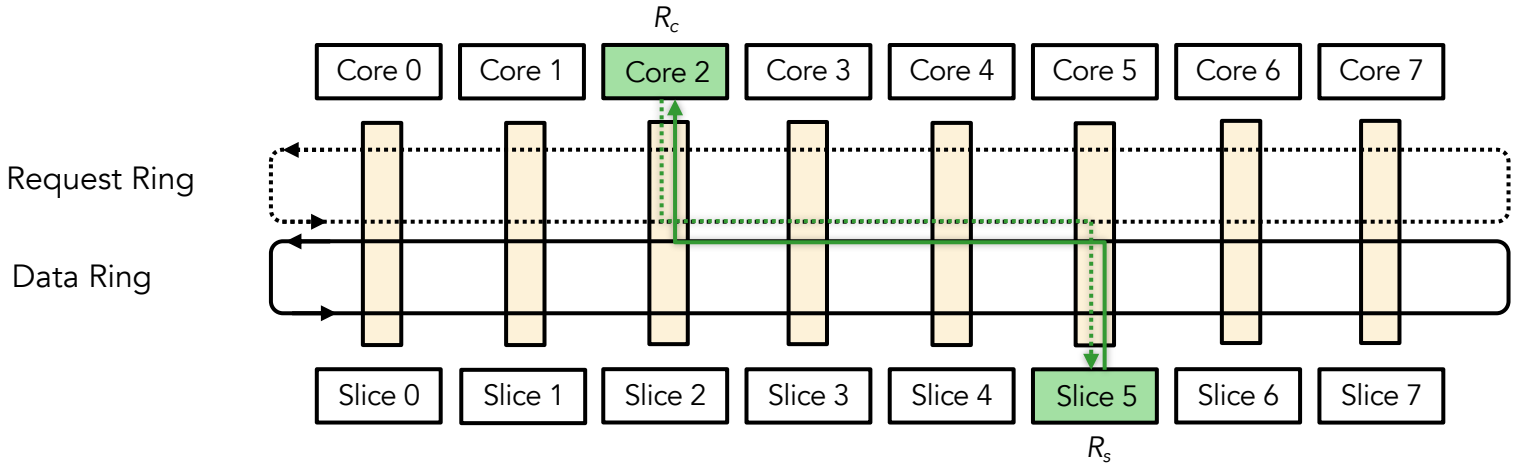
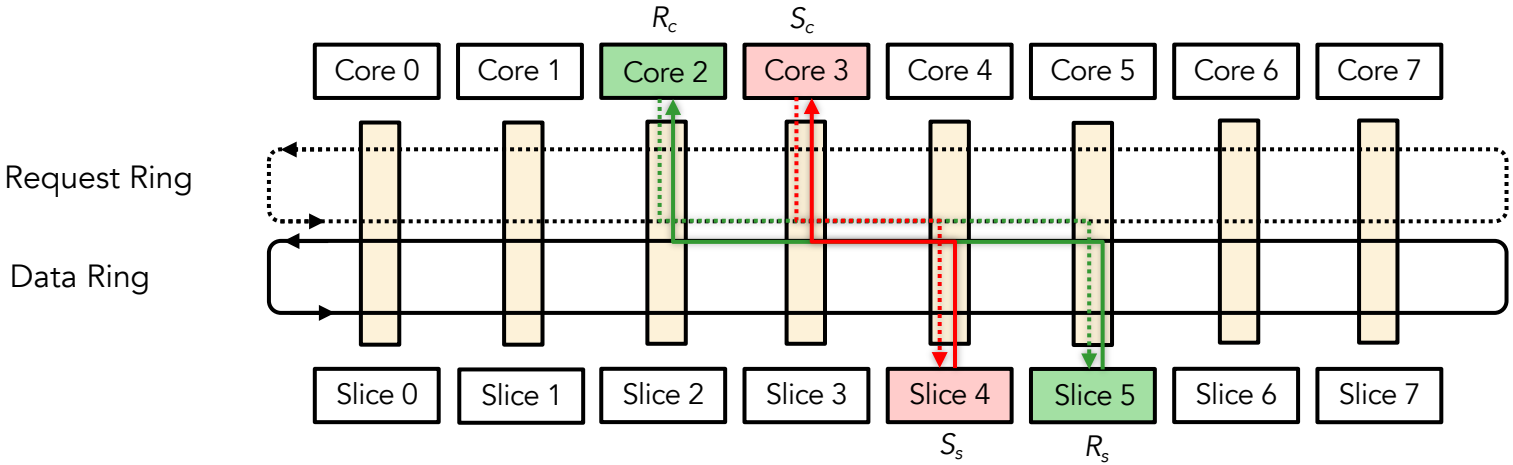




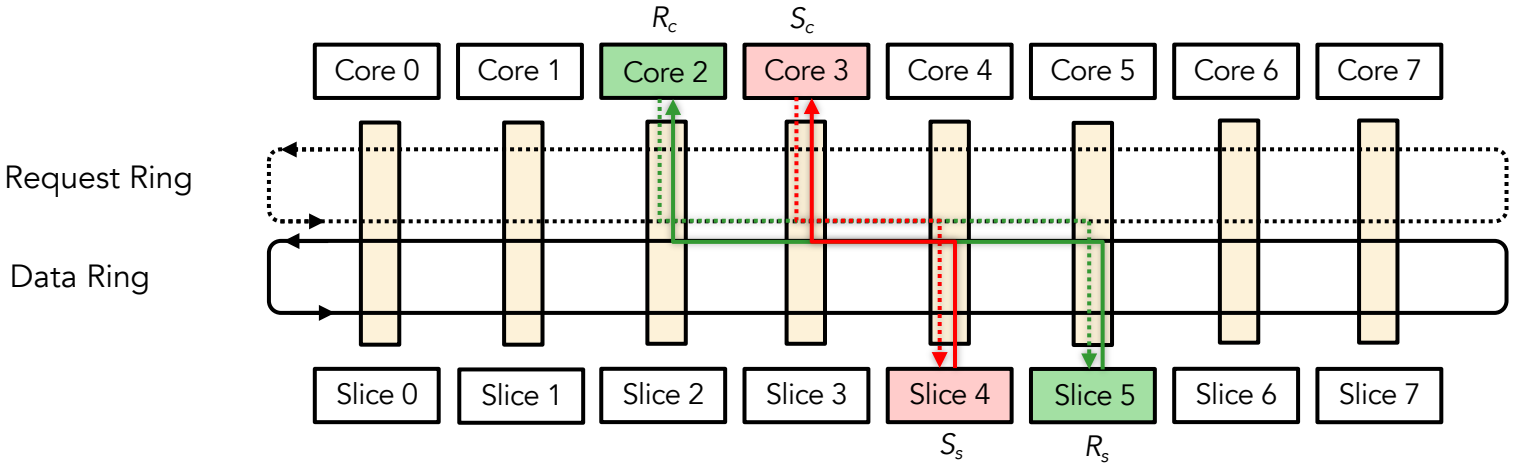
Distributed Arbitration

- Receiver envelops the sender = no contention



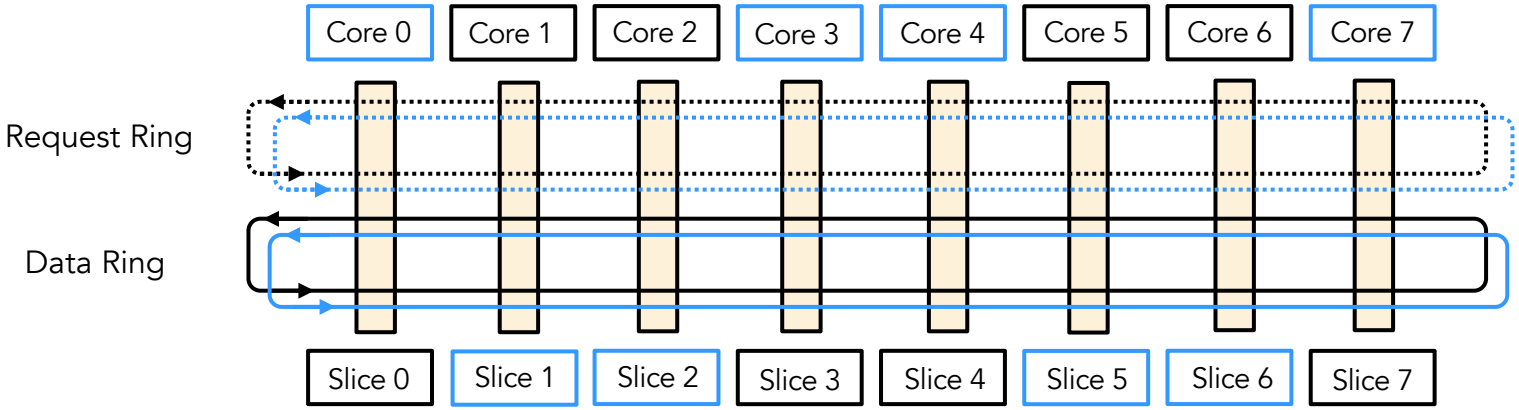
Distributed Arbitration

- Receiver envelops the sender = no contention
  - Traffic already on the ring has priority over new traffic.



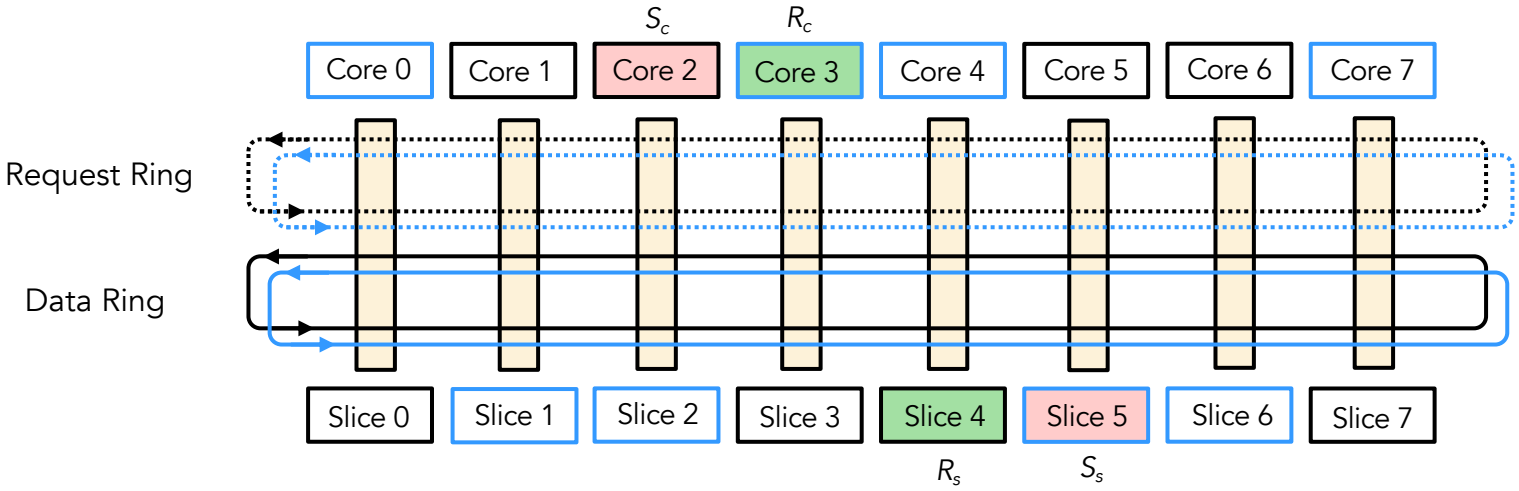
Two Lanes

- Each ring has two “lanes”, and ring stops inject traffic into different lanes depending on the cluster of its destination



Example 1

- Contention?



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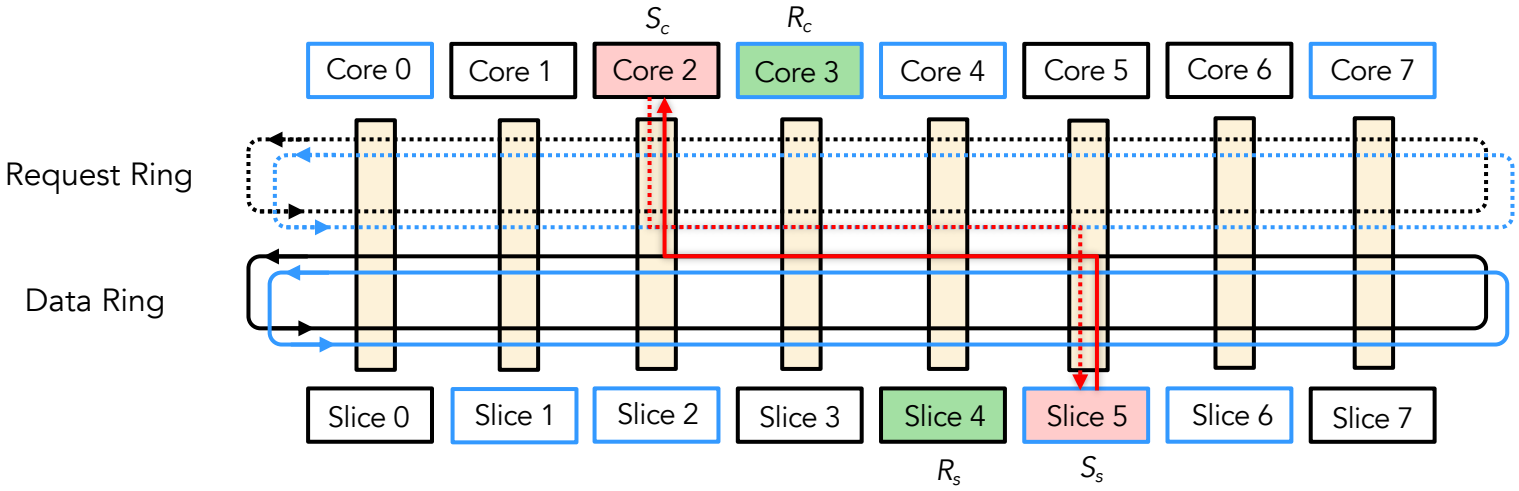

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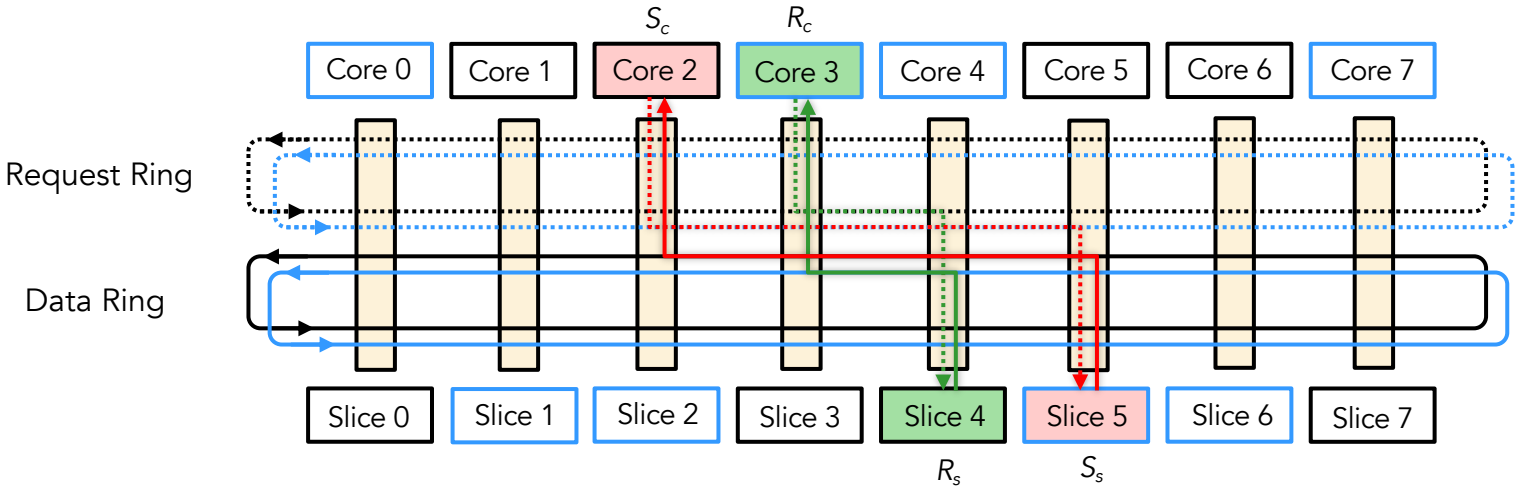
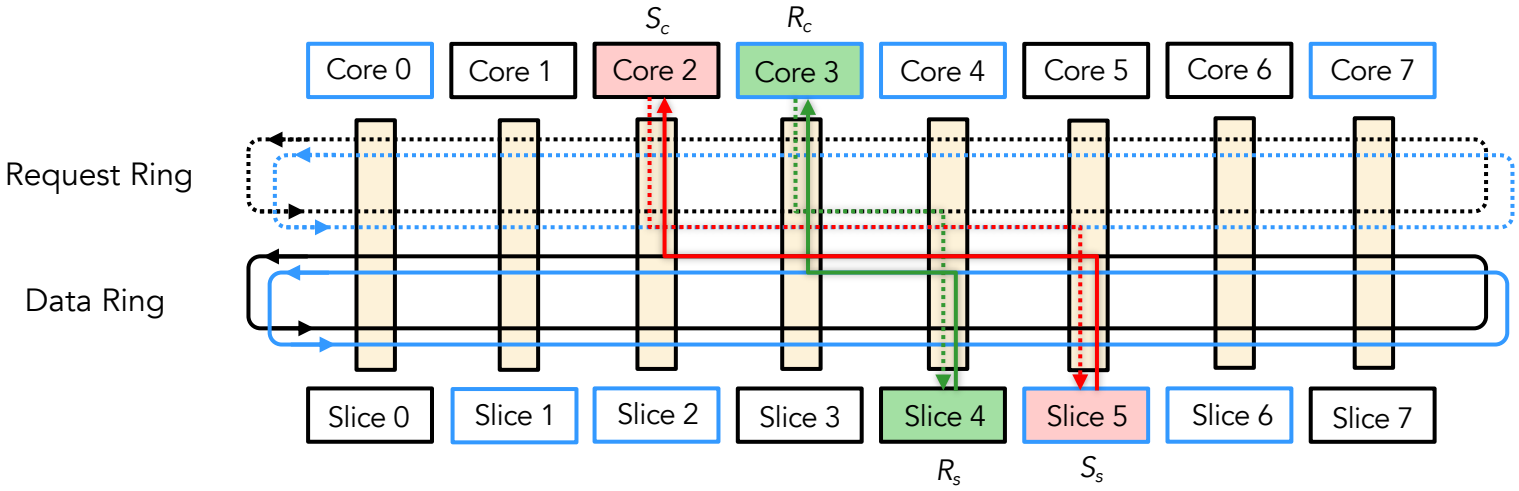


Example 1

- Contention? No, different lanes are used



Example 2

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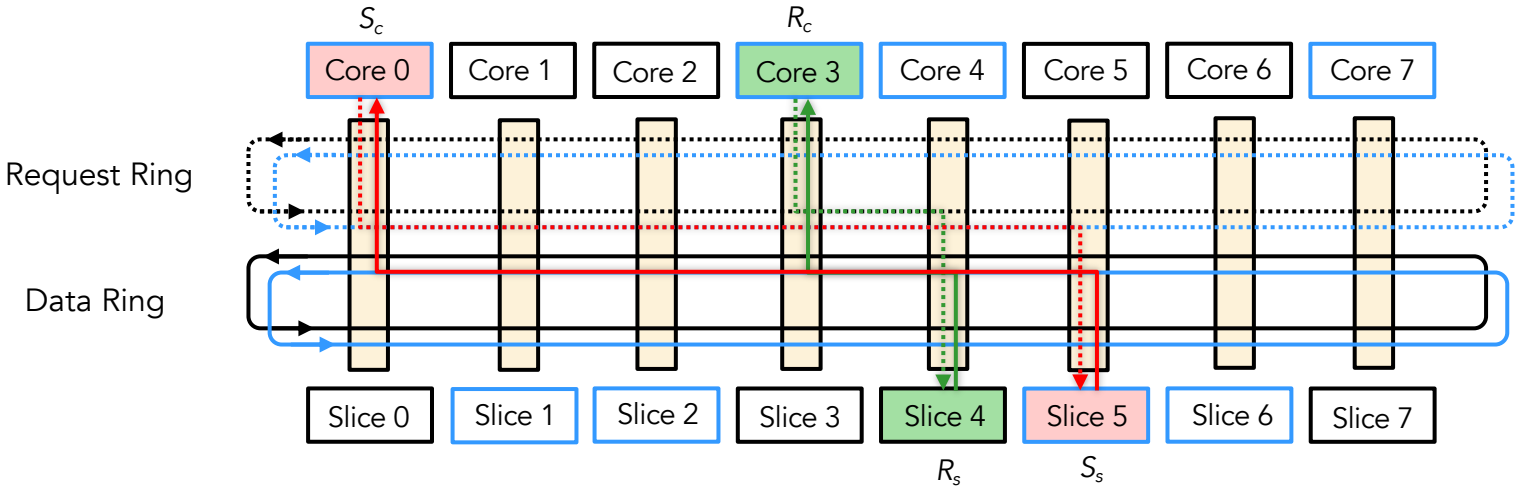
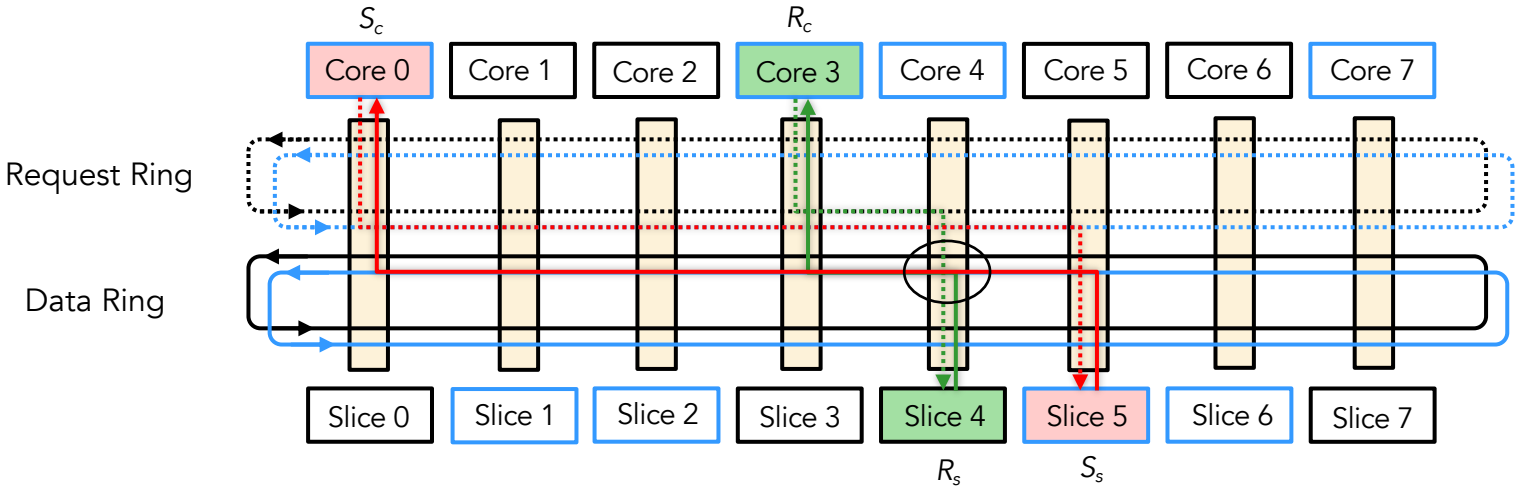


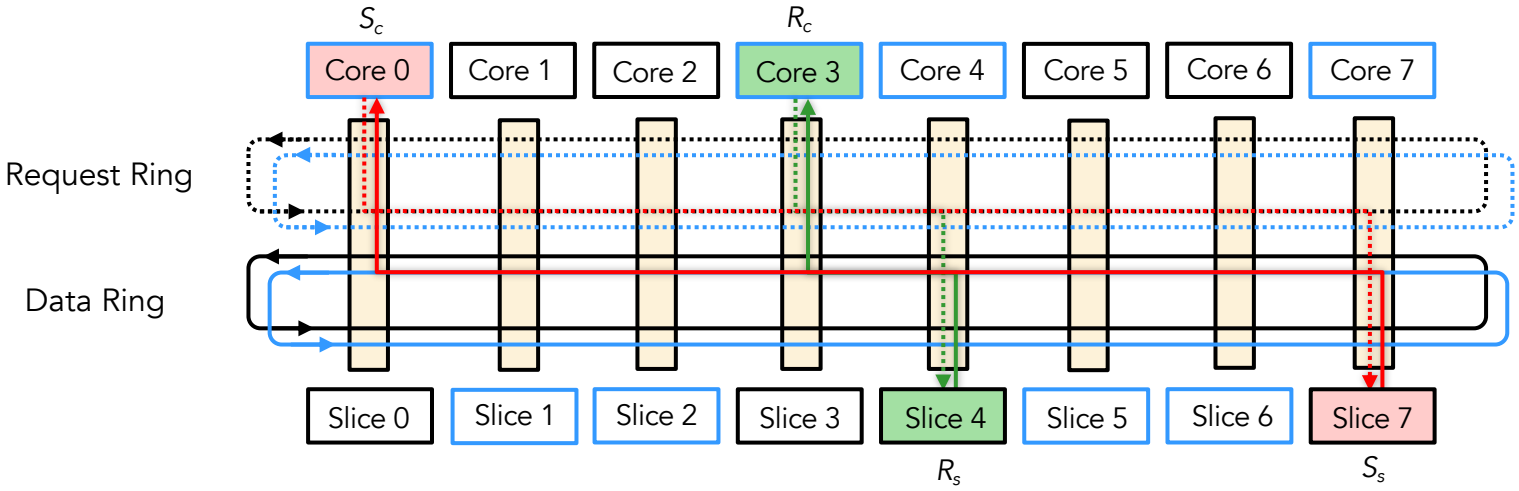
Example 2

- Contention? Yes, on the data ring!



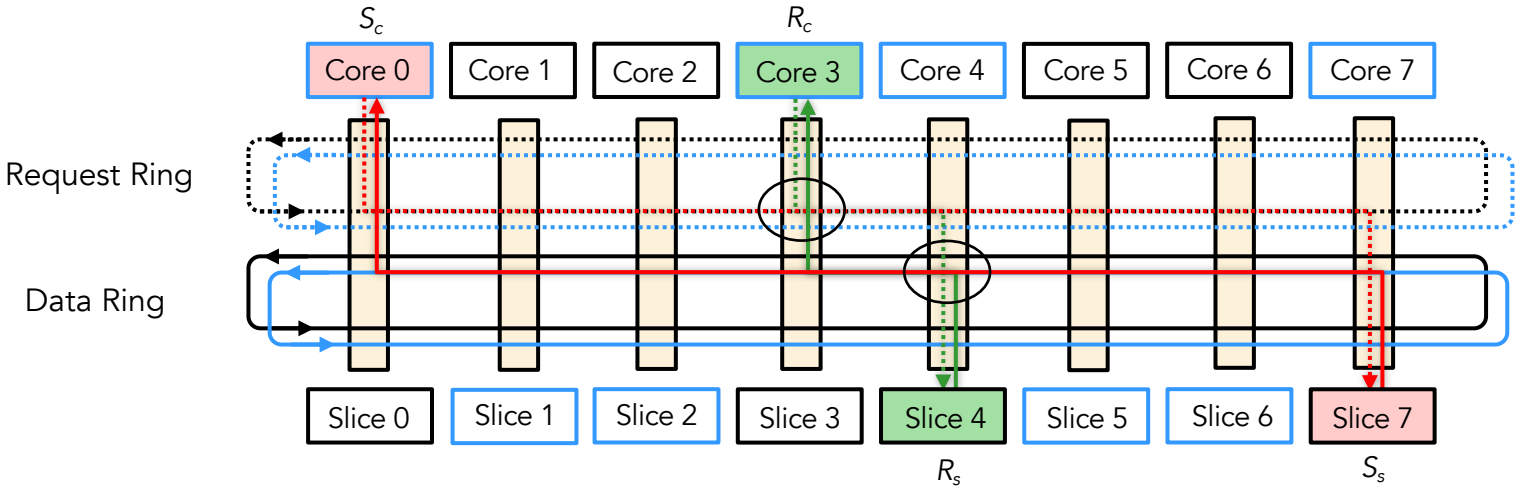
Example 3

- Contention?



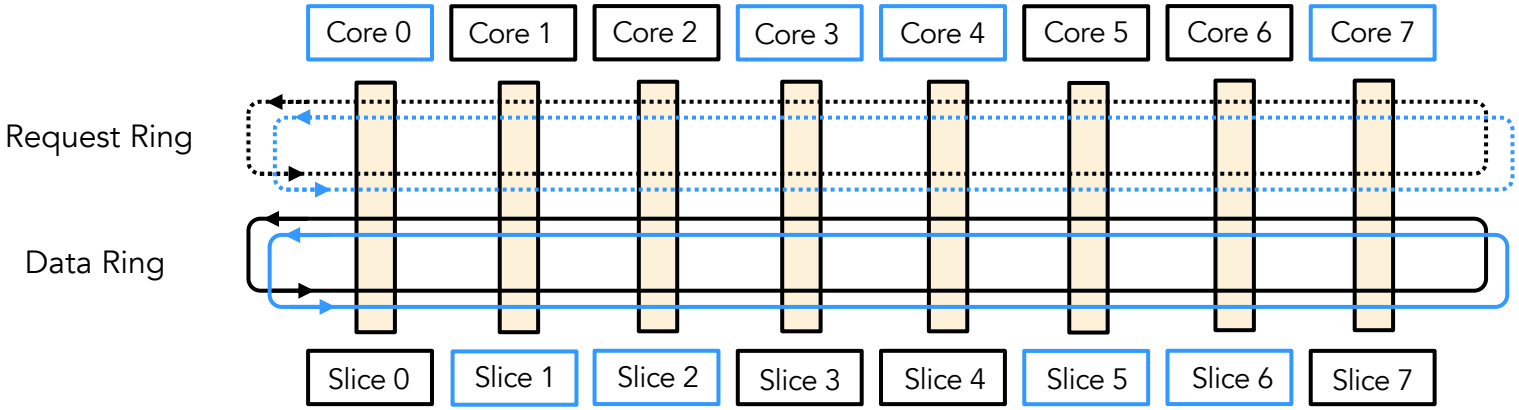
Example 3

- Contention? Yes, on the data and request rings!



Summary

- Ring contention if and only if overlapping segments + same direction + priority + same lane.



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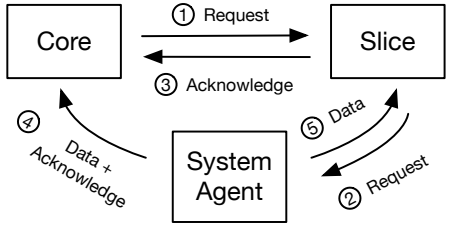

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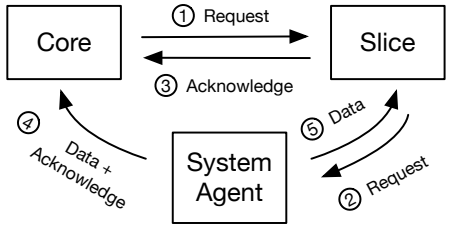
- Enabling hardware prefetchers amplifies contention.



Security Implications

- Covert channel
- Side channel attack:
  1. Side channel attack on cryptographic code
  2. Keystroke timing attack

Covert Channel

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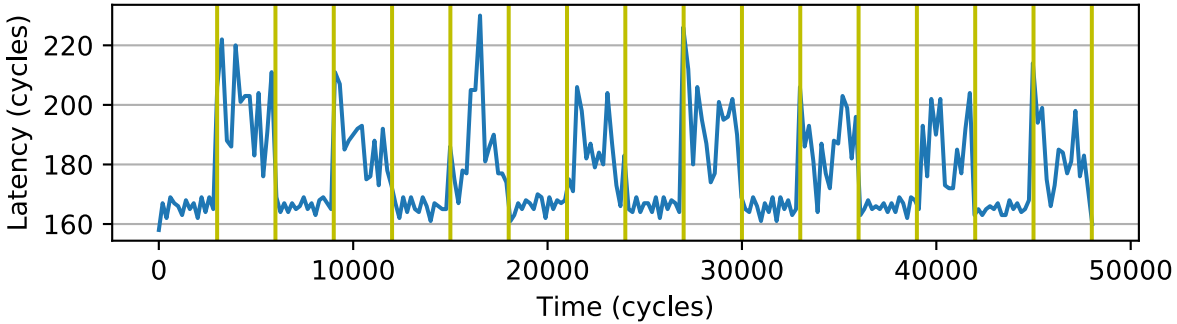

Sender sending 010101…

- Peaks are ones
- Valleys are zeros

Covert Channel

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- Largest to date for channels that do *not* rely on shared memory!

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    E1();
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More details in the paper

RSA square-and-multiply

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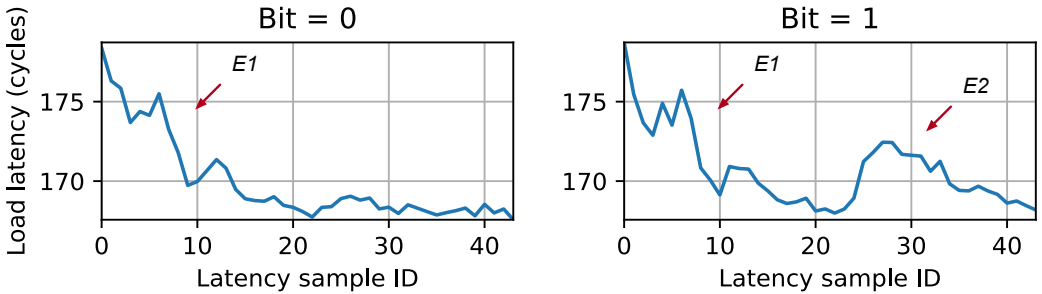


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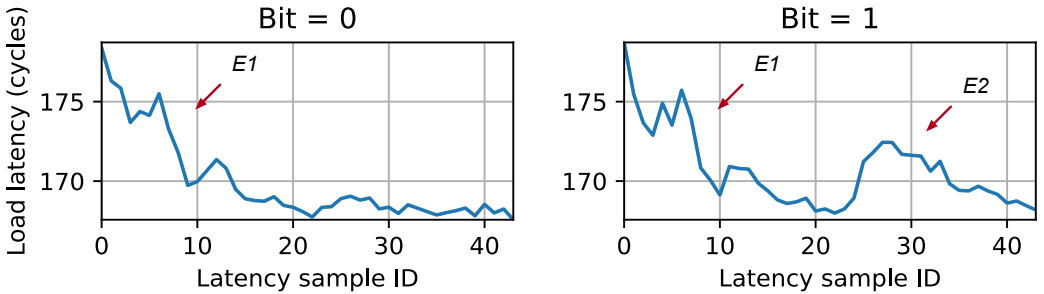
[1] $R_c = 2$, $R_s = 1$, $S_c = 5$

RSA square-and-multiply

- What the attacker (receiver) sees (average over 100 traces) [1]:




```
foreach bit b in key k do
    E1();
    if b == 1 then
        E2();
```

- We trained an SVM classifier to distinguish traces where bit=0 from traces where bit=1. Accuracy = 90%.

[1] $R_c = 2$, $R_s = 1$, $S_c = 5$

Keystroke timing attack

- **Goal**: detect *when* keystrokes occur to extract precise inter-keystroke timings (which can be used to leak passwords).

Keystroke timing attack

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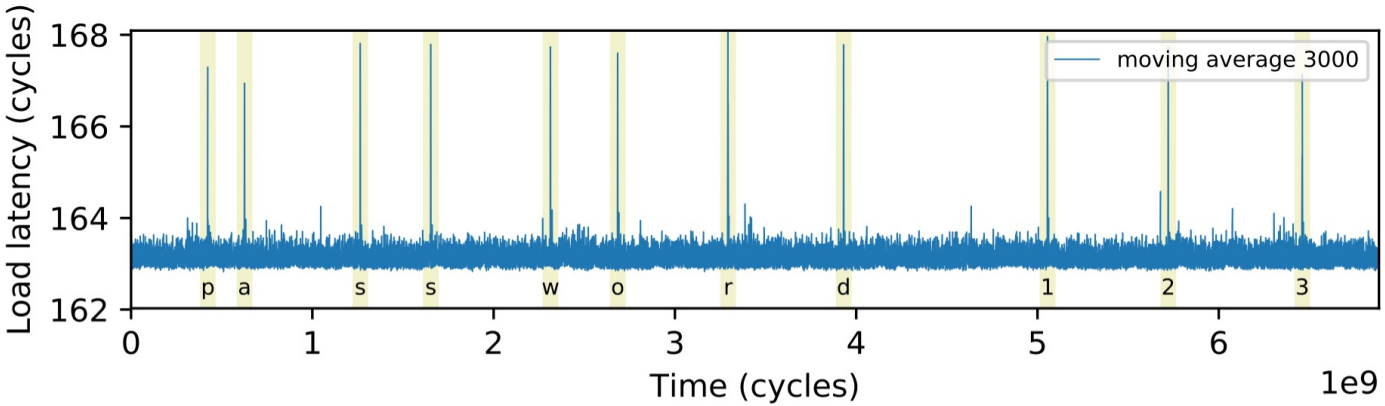
- Does processing a keystroke cause ring contention?

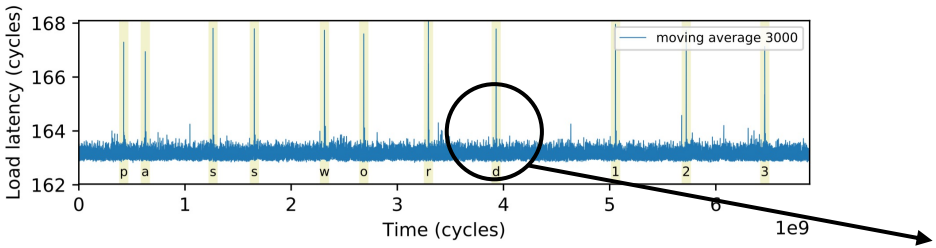
Keystroke Timing Attack

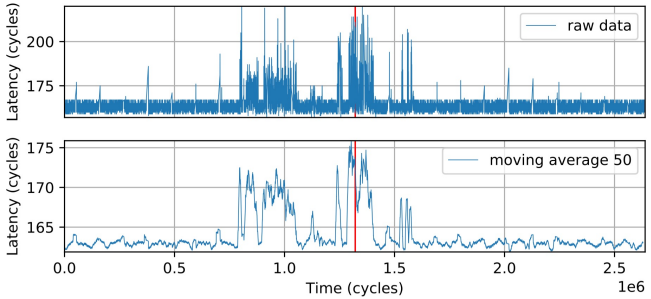
- What the attacker (receiver) sees:



Keystroke Timing Attack

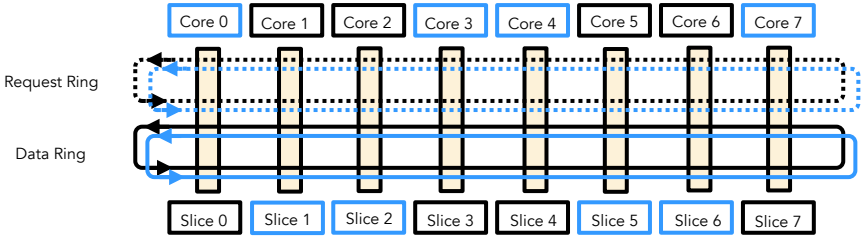
- What the attacker (receiver) sees:

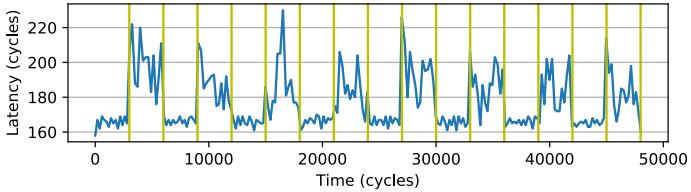


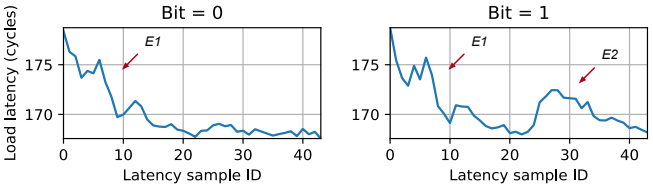


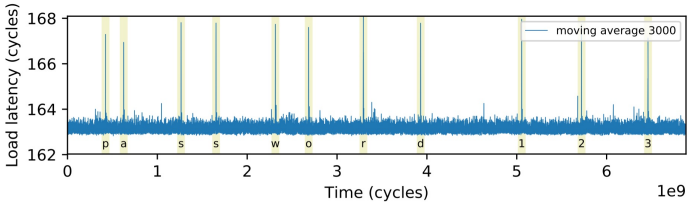
More details in the paper

Conclusion









https://github.com/FPSG-UIUC/lotr